

Josephson Junction Tuning Described by Depinning Physics

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(Received 21 July 2025; accepted 7 October 2025; published 4 November 2025)

Superconducting quantum computers leverage superconducting qubits, systems with well-defined energy levels, the spacing of which is determined by the properties of embedded Josephson junctions. Indeterminacy of Josephson junction manufacturing limits large-scale superconducting circuits; however, junction-by-junction tuning affords the possibility of an order of magnitude improvement of determinacy—although the origin of this tuning effect is uncertain. Understanding how tuning techniques may physically modify the tunnel barrier of a Josephson junction is important and will enable these techniques to be optimized. We develop a model of junction tuning based on depinning theory to interpret a phase diagram of the tuning rate. We extract the dependence on temperature, time-varying voltages, and oscillation frequency. Comparing the effect of junction tuning on room-temperature I - V 's, electrical breakdown, and frequency of higher-energy levels of transmon qubits indicates that the tuning process leaves the barrier thickness unchanged but modifies its composition.

DOI: 10.1103/xkqs-grnd

Quantum computers with high qubit count, low error rates, and error-correcting protocols promise new computational capabilities. Processors comprised of superconducting qubits are a leading platform for utility-scale quantum computation [1–3], but building these at scale and with high quality poses many challenges. One component which poses manufacturing difficulties is the Josephson junction (JJ). These are most often based on stacks of Al/ AlO_x /Al and are typically made by shadow angle evaporation [4] where a bottom layer of thin-film aluminum is oxidized before being coated by a second layer of aluminum. State-of-the-art variation in as-fabricated JJs currently limits junction resistance accuracy to $\approx 2\%$ [5–10]. The problem of junction variation will likely be exacerbated in larger wafers necessitated by larger processors and by the use of long-range couplers [11]. Simulations show that current manufacturing accuracy is insufficient to build large, high-quality, quantum processors [5,8,10]. Improvements to frequency assignment enabled by tuning protocols have been shown to improve processor yield experimentally [9]. Not only are junctions challenging to make with tight tolerance, but their properties change over time after their

manufacture in a process known as aging [12], which complicates processor design. In order to address this variation a family of techniques which allow postmanufacture parameter adjustment have been developed including modifying the junction by laser irradiation [5,13], electron beam irradiation [14], and alternating bias-assisted annealing [15]. These techniques, referred to here as tuning, cause the resistance of junctions to increase only.

In this Letter, we explore the voltage-temperature-frequency space of alternating bias assisted annealing, facilitated by a simplified lock-in tuning technique adapted from [15]. We interpret the resultant phase diagram using depinning theory, which applies to a wide range of systems in which there is an interplay between disorder, temperature, and applied stresses. This is seen in domain walls in magnets, the movement of vortices in superconductors, charge movement in Josephson junction arrays, dislocation movement, crack formation, and even the formation of avalanches in sand piles [16–20]. We find good agreement between our depinning model and the three-dimensional phase diagram. We compare tuned and untuned junctions measuring tunneling I - V curves, breakdown voltages, and Josephson harmonics [21].

We build a setup shown schematically in Fig. 1(a), where we connect a JJ in series with a load resistor, creating a potential divider, and connect this circuit between the output ports of a Zurich Instruments MFLI lock-in amplifier. Measuring the voltage drop across either of these elements allows us to infer the resistance of the JJ, the property we optimize in this process. We can control both the amplitude and the frequency of the ac voltage output from the lock-in amplifier. The sample containing JJs is

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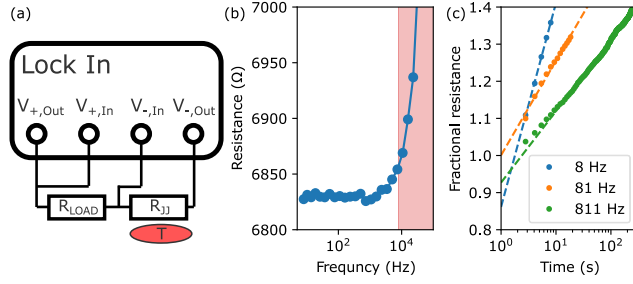


FIG. 1. (a) A schematic of the experimental setup showing a lock-in amplifier applying a voltage across a load resistor and a JJ in series. A heater controls the temperature of the JJ. (b) Resistance as a function of the frequency of the lock-in amplifier. Above ~ 8 kHz, the nominal resistance of the junction increases rapidly with frequency, a region we omit from study. (c) Three example tuning curves where the fractional resistance of the JJ (i.e., resistance normalized to that at the start of the protocol) against the elapsed time in the protocol performed at 80°C and a tuning voltage of 0.95 V. Dashed lines are a fit of the data to Eq. (1).

placed on a Peltier heating stage to control the temperature of the JJ during this process. JJs are fabricated as per the process described in Ref. [22]. Here Dolan bridge junctions with an area of $\sim 84\,000\text{ nm}^2$ are fabricated by shadow evaporations before and after a static oxidation step. An atomic force micrograph of a typical junction is shown in Supplemental Material [23], which includes Ref. [24].

We measure the resistance of the JJ as a function of the lock-in frequency [Fig. 1(b)] and find that we measure a constant value up to a frequency of ~ 8 kHz, when the measured resistance increases. This increase in resistance is a measurement artifact due to RC filtering based on a computed cutoff frequency of ~ 40 kHz, with most capacitance arising from coaxial cabling—a series resistance of $15\text{ k}\Omega$ ($10\text{ k}\Omega$ load and $\sim 5\text{ k}\Omega$ junction resistance) together with 3 m of BNC cables (typical capacitance of $\sim 80\text{ pF/m}$) gives an RC frequency of 44 kHz . We confine our frequency operating window to frequencies of 1 kHz and below to ensure we infer the correct resistances of the JJs.

In Fig. 1(c), we show how resistance changes during the tuning protocol for three frequencies: 8 , 81 , and 811 Hz . We fit these tuning curves phenomenologically to a model where the resistance increases logarithmically with time:

$$R(t)/R_0 = a \log(ct), \quad (1)$$

where R_0 is the resistance at the start of the protocol and both a and c are fit parameters, with a relating to the speed of tuning. We find this model fits all measured tuning curves well and that tuning increases in speed with decreasing frequency. On some occasions, not shown in Fig. 1, the junction fails during the tuning process, becoming a short circuit. The rate of junction failures

for a given process is another parameter we explore. We show that the behavior (speed and failure rate) of junctions undergoing voltage tuning can be understood qualitatively in terms of depinning theory.

The classic picture of depinning theory as applied to disordered media invokes two phases: a pinned static phase where the system is in a relaxed local minimum and a sliding phase where local regions or domains within the system have a nonzero average velocity [25,26]. The domains of depinning theory are a general concept, which may sometimes be instantiated by magnetic domains specifically, but this commonality in terminology is not fundamental. For example, domains may similarly be regions of sand grains or any other type of effective degree of freedom that “depins” in a disordered system. In the pinned phase, any static or oscillating field can induce local microscopic changes, which can act as a dissipation channel [27], but not large-scale movement or restructure. Above some threshold applied field (the “depinning threshold”), the movement of these local domains has some finite average velocity and can ultimately lead to avalanche behavior.

We consider the junction dielectric to host domains which are trapped local minima. These domains may be 0D vacancies or interstitials, 1D chains of such vacancies, or 2D boundary regions of lower-density amorphous material or something else—the depinning treatment here is agnostic to the underlying microphysics. Applying sufficient field or temperature can move these domains, surmounting some effective potential barrier. Following Nattermann *et al.* [26], we define the depinning temperature T_P , where the thermal energy is equivalent to the barrier height. The depinning voltage V_P is the point at which there is sufficient applied field for domains to continuously move through the material, resulting in an avalanche.

The regions of interest in a generic depinning theory are illustrated in Fig. 2(a). The linear response or “running” region (blue shaded area) applies for constant fields greater than the temperature-dependent depinning voltage $V_P(T)$. Any constant applied field less than this will not result in a significant change in the structure of the material; it will be “pinned” (the red shaded area). The zero temperature limit of $V_P(T \rightarrow 0)$ is the threshold voltage V_{th} .

The general depinning threshold [$V_P(T)$] which separates these two regions can be defined for temperature T and voltage V by the relation

$$T = T_P \frac{V_{th}}{V} \left(1 - \frac{V}{V_{th}} \right)^{1/\mu}, \quad (2)$$

where μ is a constant which depends on the effective dimensionality of the elastic object (for one- to two-dimensional domains in a 3D medium, it can be approximated to 1) [26,28].

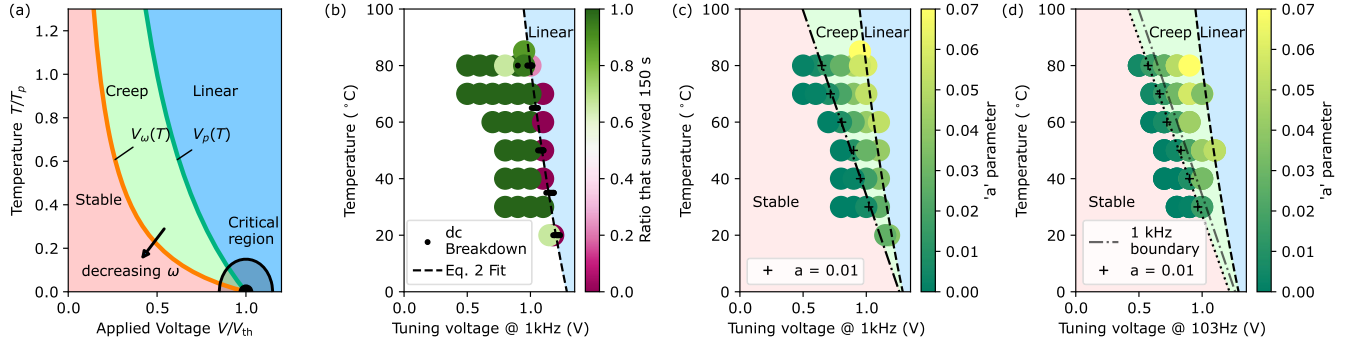


FIG. 2. (a) Generic phase diagram for depinning theory, showing three operating regimes, where the creep regime is where tuning occurs. (b) Threshold voltage phase diagram as a function of tuning voltage and temperature. Measurements of the fraction of junctions failing during processing show this boundary. Overlaid are dc measurements of breakdown which follow the same boundary separating the creep and linear regimes. These data are fit by Eq. (2) (c) 1 kHz and (d) 103 Hz resistance tuning speed phase diagram. The parameter a from Eq. (1) is shown using a color scale. The boundary between the creep and linear regime found by fitting dc breakdown in (b) is shown in both phase diagrams, as is a straight line fit to points where the interpolated value of a is 0.01 showing the stable or creep boundary. In (d), we show the boundary for both 1000 and 103 Hz, showing that with decreasing frequency the boundary has moved to lower voltages and temperatures.

When an oscillatory field is applied, a third regime is formed in the phase diagram. The so-called “creep” region [green region in Fig. 2(a)] is the region in which domains can most easily move under application of an oscillatory field. In the creep region, the oscillating field results in hysteretic behavior [17,29].

A general expression for the creep threshold $V_\omega(T)$ is difficult to derive without an explicit microscopic model. Nattermann *et al.* suggested [26,28] this boundary can be found by modifying Eq. (2), replacing $T_p \rightarrow T_p/\Lambda$ in the adiabatic limit. In this case, $\Lambda = \ln(1/\omega_0\tau)$ depends on the oscillation frequency ω_0 and the characteristic timescale τ required for a domain to overcome the barrier to move from its local equilibrium. In what follows, we find this significantly overestimates the shift due to variation in ω_0 for sensible estimates of τ , suggesting that a more rigorous treatment is required that goes beyond the adiabatic approximation.

Interpreting the junction tuning results in terms of depinning suggests (a) if $\omega_0\tau < 1$, the creep region is larger for lower frequencies, and (b) in the creep regime, there is a linear movement of defects without leading to full avalanche. This explains why lower frequencies result in greater resistance shifts for fixed values of temperature and voltage amplitude. At some low-frequency limit, we anticipate this trend stops, as domain movement saturates before the field polarity is reversed, presenting a new energy landscape to the mobile domains. We can also understand the junction breakdown in terms of the depinning avalanche process for $V > V_p(T)$, which is both temperature and local microstate dependent.

To explore our interpretation, we tune junctions with varying voltage and temperature at frequencies of both 1 kHz and 103 Hz. For each parameter set, we tune at least three junctions. We fit each of these tuning curves to Eq. (1)

and extract the speed parameter a . We also compute how many junctions fail prior to 150 s of tuning process. We present these data as a function of temperature and voltage amplitude [Fig. 2(b)]. A clear boundary is observed at a tuning voltage of $\gtrsim 1$ V. This boundary is matched by dc measurements of breakdown voltage performed at varying temperature. We, therefore, associate this boundary with the depinning threshold $V_p(T)$ and fit the dc breakdown to Eq. (2).

We continue to map out the phase diagram by measuring the tuning “speed” parameter a in Eq. (1). Operating at 1 kHz, we vary the temperature and voltage amplitude of the tuning process. In Fig. 2(c), we plot a , finding a similar boundary, now at a lower voltage, consistent with the expected behavior of $V_\omega(T)$. This process is then repeated at a different tuning frequency (103 Hz) with data shown in Fig. 2(d), showing the expected increase in the creep regime with reducing frequency.

To fit the boundaries between regimes quantitatively is more difficult, as it requires estimates for τ , μ , T_p , and V_{th} and a better understanding of the relationship between depinning velocity and the tuning speed parameter. We can estimate V_{th} from junction breakdown measurements at a given temperature. Some indications for the depinning temperature can be given by observations of where the rate of thermal aging starts to increase. To give an indication of likely temperature scales, in [30–32] changes are first seen $> 125^\circ\text{C}$, and large-scale junction modification is observed at $> 400^\circ\text{C}$ in [33–36].

Using the approach [26,28] given in Eq. (2), along with a finite value of Λ , we compare to the stable and creep boundaries shown in Figs. 2(c) and 2(d). We find that, while the direction of the experimental shift with bias frequency is expected, its magnitude is actually much smaller than depinning theory would suggest (or corresponds to

unrealistically small τ —see Supplemental Material [23]). This suggests that the dynamics in the creep regime are more complicated than in previous studies of depinning.

Figure 2(a) indicates sharp lines demarking regions of the phase diagram; however, at this stage it is not clear that these boundaries are true phase transitions. The speed parameter a increases smoothly with increasing tuning voltage (the data are shown with alternate visualization in Supplemental Material [23]). This may be indicative of a second-order phase transition between the stable and creep regimes.

Mapping out this phase diagram, we have identified room-temperature working points with appreciable process speed as in Ref. [6], with an example room temperature tuning curve shown in the supplementary materials [23]. This offers multiple advantages; key among them is that junctions which are not tuned undergo no heating and associated aging, a significant benefit for processor design. The exact mechanism of the tuning, as well as the nature of the domains being depinned, is currently unknown. More detailed mapping of the phase diagram, combined with the statistics of many junctions, will provide invaluable data to compare to potential models of junction tuning.

While the depinning picture provides a qualitative description of the observed dynamics, a quantitative model is needed to understand the underlying microscopic processes. Time-dependent dielectric breakdown has been extensively studied in silica-based dielectrics [37–39] and in magnetic tunnel junctions [40] and low- k dielectrics [41,42], as well as AlO_x films [43–46]. In these materials, a variety of breakdown mechanisms have been studied, including charge trapping within the barrier, time modulation of this charge, and electric field-induced distortion of bonds in the barrier. In particular, studies of copper ion migration [41,42] have considered the influence of both convective and diffusive flux of ions. These correspond to diffusion driven by the electric field itself or by the stoichiometry gradient, respectively. This suggests a possible two-process mechanism for breakdown and tuning of Josephson junctions, namely, that breakdown is enabled by the convective movement of atoms from within the barrier in the direction of the applied field, while the tuning of the resistance at lower fields is related to the redistribution of oxygen or defects from within the barrier via diffusion—mediated by the oscillating field. To test this possibility, we investigate the average barrier characteristics before and after tuning.

Following our recent work [47], we measure the electrical breakdown of junctions by ramping a dc voltage across these junctions from 0 to 1.7 V, recording the current that flows through each junction as a function of voltage [Fig. 3(a)]. We fit the linear portion of this I - V to extract the resistance of the JJ and fit the full I - V to the Simmons model [48], fixing the area to that found by AFM measurements $8.86 \times 10^4 \text{ nm}^2$. At some voltage, the

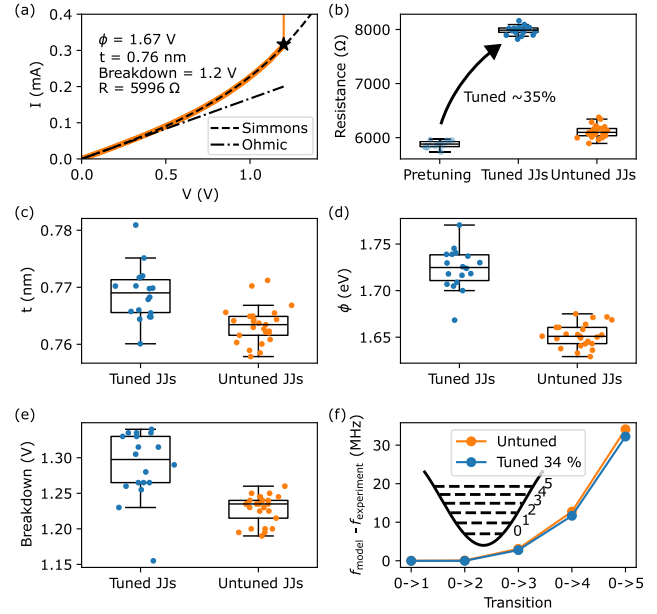


FIG. 3. Investigation of the effect of tuning on DC I - V 's, electric breakdown, and Josephson harmonics. (a) An example I - V from an untuned JJ where voltage is ramped up from 0 V. It is fit to the Simmons model to determine model nominal barrier thickness and height. It is also fit to Ohm's law to determine junction resistance. Breakdown voltage is extracted where the current suddenly jumps and is indicated with a star. (b) The resistances of the junctions which have been tuned vs those that have been subject to only the thermal history associated with tuning. The junctions are tuned an average of $\sim 35\%$ with the resistance prior to tuning shown in transparent blue markers. (c) The thickness extracted from the Simmons model, (d) the barrier height extracted from the Simmons model, and (e) the breakdown voltage are all shown comparing tuned and untuned junctions. (f) The results from Josephson harmonics experiments performed on a tuned and an untuned qubit. The difference between the frequencies predicted by the transmon Hamiltonian and those found experimentally are plotted for the different transitions.

junction fails and becomes a short circuit which is recorded as the breakdown voltage [black star in Fig. 3(a)]. We compare two sets of junctions, distinguished by their tuning, with resistances shown in Fig. 3(b). The first set of 20 junctions is tuned at 85°C with a voltage of 0.92 V targeting 30% total tuning and find an average tuning of $34.6 \pm 0.8\%$. This systematic overshoot occurs due to continued resistance changes over time, after we have hit our target value, as shown in Ref. [6]. During this process, two junctions failed. The second set of 25 junctions are fabricated on the same chip, undergo the same 85°C heating as the tuned junctions, but are not tuned by an alternating voltage. Despite undergoing no electrical tuning, they are $\sim 4\%$ higher in resistance than the junctions before tuning due to the thermal processing they undergo. This shows why a room-temperature process (as shown in Supplemental Material [23]) is advantageous, as heating chips above storage temperatures causes uncontrolled

changes in junction properties alongside the intentional tuning process.

In Fig. 3(c), we see a small increase to the average fitted barrier thickness with distributions mostly overlapping for tuned and untuned junctions. In Fig. 3(d), we see a clear increase in the barrier height for the junctions which have been tuned relative to those that have not. These results indicate that the tuning process modifies the atomic structure of the barrier more substantially than its thickness.

In Fig. 3(e), we show that on average junctions which have undergone tuning have a larger breakdown voltage, increasing by $\sim 5\%$. However, despite the increase in average breakdown voltage, the lowest breakdown voltage recorded was from a junction that had undergone tuning. The breakdown voltage is given by

$$V_{\text{BD}} = \min\{t(x, y)E_{\text{BD}}(x, y)\}, \quad (3)$$

where $t(x, y)$ is the local thickness of the barrier and $E_{\text{BD}}(x, y)$ is the local dielectric strength of the barrier. Both of these values may, in principle, vary across the barrier [49,50] and be modified by tuning. In the depinning model, we describe above domains are mobile under the application of electric fields. These fields will be the strongest at the thinnest regions of the barrier, which means that the creep rate will also be greatest at these thinnest points. Such weak points in the barrier have been suggested to contribute to nonidealities [21,50,51] and breakdown [45] of the JJs. An approach that reduces the nonidealities associated to pin holes or weak points may have advantages in homogenising the current-phase relations of junctions.

The higher-energy states of transmon qubits have recently been suggested to be sensitive to the nanostructure of the barrier in JJs [21]. In Fig. 3(f), we show the results of measuring two coaxmon qubits [52] where one qubit has had a junction tuned by 34% and the other has experienced the same thermal treatment but not been tuned. The results in Ref. [21] would suggest that by substantially modifying the barrier we might expect to see some difference to the frequencies of these higher levels. We follow the protocol from Ref. [53], treating the coaxmon as a qudit and tuning up a series of gates across the six energy levels shown schematically in Fig. 3(f). We compute the Josephson energy and charging energy using QuTip [54] by considering the first two transition frequencies and constraining them to match the results from the transmon Hamiltonian

$$H = 4E_C\hat{n}^2 - E_J\cos\hat{\phi}, \quad (4)$$

where $\hat{n}$ and $\hat{\phi}$ are the charge and phase operators, respectively, and E_C and E_J are the charging and Josephson energies, respectively [55]. The tuned (untuned) coaxmon have junction resistances of 5802 Ω (6021 Ω), charging energies of 166 MHz (168 MHz), and Josephson energies of 23.2 GHz (22.2 GHz). In Fig. 3(f), we show the difference between the measured transition frequencies and

the computed transition frequencies for the different qudit states for both a tuned and untuned coaxmon. We find the relative difference in model and experiment discrepancies for tuned and untuned junctions to be small relative to lab-to-lab variation or even qubit-to-qubit variation from a single institute presented in Ref. [21] and, therefore, conclude that the tuning process has not substantially modified the Josephson harmonics in this instance. Statistical studies comparing multiple tuned and untuned qubits may allow small effects to be resolved in future studies.

By mapping out the voltage-temperature-frequency phase diagram of tuning under oscillatory bias, we have shown that the tuning process is qualitatively described by depinning theory. The domains within the amorphous oxide barrier creep between local minima driven by both temperature and the oscillating field. Depinning theory by itself does not point to a particular origin of these local domains, as it is consistent with small-scale defects [56], movement of grain boundaries [57], or other microscopic models [27]. Nonetheless, by interpreting the results in terms of depinning theory, the working point can be chosen to improve the junction tuning protocol, choosing how deeply into the creep region one wishes to operate. We find a set of parameters that allow junction tuning at room temperature with appreciable speed, where untuned junctions are also not subject to heating and associated modifications.

We show that tuning modifies not only the resistance of the junctions, but also the barrier height in the junction and the breakdown voltage of the junctions. We contrast this to a measurement of “Josephson harmonics” which appear unchanged comparing tuned and untuned junctions. The interpretation in Ref. [21] suggests that deviations in these harmonics can be ascribed to the thinnest points of junctions. Taken together, our measurements suggest that the depinning process modifying the junction resistance is not simply “filling in” the thinnest points of barriers but fundamentally modifies the junction microstructure.

Acknowledgments—We extend our thanks to the OQC fabrication team for discussions relating to this work, the fabrication of junctions, and AFM measurements of junction area. We acknowledge the OQC hardware team for developments across the stack which enabled these measurements. The authors thank Dave Pappas and Simon Brown for useful discussions. The authors thank Peter Leek and Jonathan Burnett for reviewing this manuscript. Computational resources were provided by the Australian National Computational Infrastructure facility (NCI). We thank the Royal Holloway University of London SuperFab Facility for their support.

Data availability—The data that support the findings of this article are not publicly available because they contain commercially sensitive information. The data are available from the authors upon reasonable request.

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