

Constant-depth fan-out with real-time feedforward on a superconducting quantum processor

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When using unitary gate sequences, the growth in depth of many quantum circuits with output size poses significant obstacles to practical quantum computation. The quantum fan-out operation, which reduces the circuit depth of quantum algorithms such as the quantum Fourier transform and Shor's algorithm, is an example that can be realized in constant depth independent of the output size. Here, we demonstrate a quantum fan-out gate with real-time feedforward on up to four output qubits using a superconducting quantum processor. By performing quantum state tomography on the output states, we benchmark our gate with input states spanning the entire Bloch sphere. We decompose the output-state error into a set of independently characterized error contributions. We extrapolate our constant-depth circuit to offer a scaling advantage compared to the unitary fan-out sequence beyond 25 output qubits with feedforward control, or beyond 17 output qubits if the classical feedforward latency is negligible. Our work highlights the potential of midcircuit measurements combined with real-time conditional operations to improve the efficiency of complex quantum algorithms.

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I. INTRODUCTION

Using the outcome of midcircuit measurements to conditionally apply quantum gates to a subset of qubits in a quantum circuit is often referred to as adaptive control. Adaptive control enables quantum circuits, which are more efficient than static ones, or even ones that are otherwise unattainable [1]. Early experiments showed the role of measurement-based adaptive control in applications including qubit initialization [2,3], quantum teleportation [4–9], and state stabilization [10–13]. Entering the noisy intermediate-scale quantum (NISQ) era, adaptive circuits raise interest in their potential to reduce the circuit depth of quantum algorithms [14–16]. Compared to unitary sequences, protocols with adaptive circuits could achieve lower circuit depths [1] and show favorable error scaling in tasks such as CNOT gate teleportation and Greenberger-Horne-Zeilinger (GHZ) state preparation [17].

Constant-depth quantum fan-out is a powerful protocol enabled by adaptive control [14,18]. Quantum fan-out increases the parallelization of instructions and allows the efficient implementation of quantum computing tasks, such as constant-depth quantum Fourier transform [18], constant-depth extraction of Hamming weights [18], and polylogarithmic-depth Shor's algorithm [14]. Recently, a 1-to-3 quantum fan-out gate was demonstrated with superconducting qubits [19]. The fan-out operation was applied to the computational basis states, and the performance was limited by measurement-induced cross dephasing.

Here, we present a constant-depth quantum fan-out gate with real-time feedforward and up to four output qubits. Adding to the above experiment, we realize quantum fan-out on input states parameterized over the Bloch sphere, and thoroughly decompose the error of the sequence. In Sec. II, we introduce the quantum fan-out gate sequence and describe its implementation on a 17-qubit superconducting quantum processor [20]. In Sec. III, we present our main results. We start by examining the density matrices and the multiqubit Pauli operator expectation values of two example output states, showing that the fan-out gate yields the expected output. Then, we prepare the input state in a set of states parameterized by polar and azimuthal angles on the Bloch sphere and analyze the output states

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with quantum state tomography. Furthermore, we investigate the scaling of the fan-out gate error with the number of output qubits and decompose the measured error into individually characterized error sources. To understand the gate performance in the absence of the feedforward delay set by the latency of the control electronics, we replace the physical application of a feedforward control pulse with a rotation of the Pauli reference frame in postmeasurement analysis. We observe a reduction in the measured error in agreement with the contribution expected from qubit decoherence during the idling time required to instantiate the feedforward pulses. Finally, we compare the performance of the constant-depth fan-out circuit with the static, unitary fan-out circuit. Extrapolating the error scaling suggests that the constant-depth circuit yields a benefit beyond 25 output qubits with feedforward control, or beyond 17 output qubits if the electronics latency can be reduced to negligible levels.

II. CIRCUIT AND IMPLEMENTATION

We implement a constant-depth quantum fan-out gate with n output qubits based on a teleportationlike protocol with GHZ states [14]. The protocol requires $3n - 2$ qubits arranged in a linear array with nearest-neighbor coupling. The first qubit in the array Q^{in} carries the input state, and the rest of the qubits can be divided into $(n - 1)$ groups of three qubits $\{Q_i^a, Q_i^b, Q_i^c\}$, see Fig. 1. The protocol is executed in four time steps. In the first step, we simultaneously **prepare** Q^{in} in the state $\alpha|0\rangle + \beta|1\rangle$ and the three qubits in each group in the GHZ state. In the

second step, we execute controlled-NOT (CNOT) gates followed by a Hadamard gate to **entangle** both the input qubit and its neighboring qubit, as well as qubit pairs across the boundary of qubit groups for Bell measurements. In the third step, we **measure** all pairs of the qubits entangled in the previous step, yielding the measurement results in the computational basis $(z_1, x_1, \dots, z_{n-1}, x_{n-1}) \equiv (\mathbf{z}, \mathbf{x})$, where z_i and x_i are the results of the first and second qubit in each Bell basis measurement. In the fourth step, we use classical control instruments to **feedforward** recovery pulses $R_q(\mathbf{z}, \mathbf{x})$ to the qubits. $R_q(\mathbf{z}, \mathbf{x})$ is a product of conditional X and Z gates, where the application of the X gate depends on the parity of all x -type qubit results $\{x_m\}$ for qubit indices smaller than or equal to the output qubit considered, i.e., $m \leq q$, and the application of the Z gate is conditioned on the result of the closest z -type qubit result z_q . An exception applies to the last recovery pulse $R_n(\mathbf{z}, \mathbf{x})$, where the conditional Z gate is not needed. $R_q(\mathbf{z}, \mathbf{x})$ can be expressed as

$$R_q(\mathbf{z}, \mathbf{x}) = \begin{cases} Z^{z_q} \prod_{m=1}^q X^{x_m}, & 1 \leq q \leq n-1 \\ \prod_{m=1}^{n-1} X^{x_m}, & q = n. \end{cases} \quad (1)$$

In the absence of errors, the output qubits are deterministically prepared in the target state $\alpha|0 \dots 0\rangle + \beta|1 \dots 1\rangle$.

We apply the gate sequence to a one-dimensional chain of ten transmon qubits of a 17-qubit superconducting quantum processor [20] (see sample and setup details in Appendix A). With ten qubits, we realize a quantum fan-out with four output qubits. Single-qubit gates are performed with DRAG pulses [21] and virtual Z rotations [22]. The CNOT gate is implemented with a flux-activated net-zero controlled- Z (CZ) gate [23] and single-qubit rotations (see gate sequence and time budget in Appendix B). The simultaneous readout is realized using frequency-multiplexed readout tones selectively applied to the readout resonators of the target qubits [24]. The mid-circuit readout response is integrated and classified in real time with an FPGA embedded in each control electronics, and the readout result of each qubit, as a single-bit value, is forwarded to a central control unit. The set of all readout results is interpreted with programmable lookup tables to one 2-bit index per output qubit, uniquely defining the feedforward pulse to be applied. The indices are forwarded to the drive instruments of the output qubits, which apply the single-qubit rotation pulses accordingly. During the classical processing time, we perform Carr-Purcell-Meiboom-Gill (CPMG) dynamical decoupling pulses [25,26] on every output qubit to mitigate the decoherence error from low-frequency noise. The whole sequence lasts 1888 ns independent of the output qubit number, with a 800-ns latency required of the classical processing for the feedforward control (see the breakdown of time budget in Appendixes A and B).

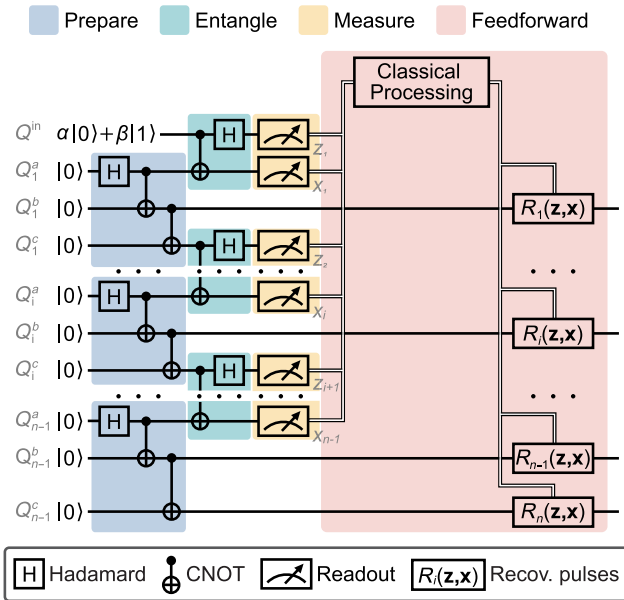


FIG. 1. Circuit diagram of the constant-depth quantum fan-out gate. Background colors mark the different steps of the circuit.

III. FAN-OUT GATE CHARACTERIZATION

We execute the feedforward-based 1-to-4 fan-out gate with input state $|1\rangle$ and characterize the output state using quantum state tomography [27]. We compare ρ to the ideal density matrix ρ_{ideal} (black wireframes) and extract an experimental output state fidelity $F = (\text{Tr} \sqrt{\sqrt{\rho} \rho_{\text{ideal}} \sqrt{\rho}})^2 = 0.797$, see density matrix ρ obtained using maximum-likelihood estimation in Fig. 2(a). Similarly, we execute the experimental sequence

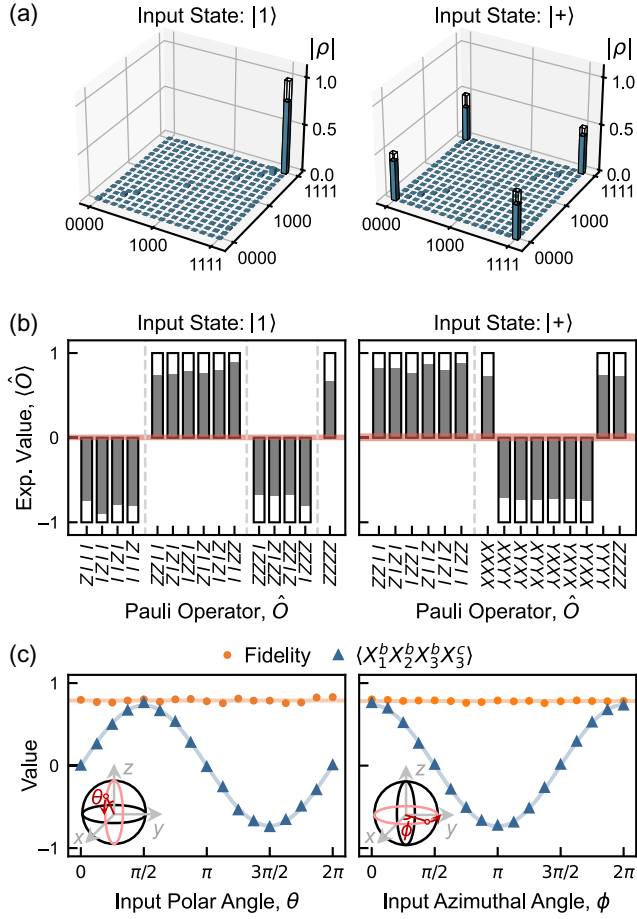


FIG. 2. (a) The absolute value of the maximum-likelihood estimation of density matrix ρ when the input qubit is prepared in the $|1\rangle$ (left) and $|+\rangle$ (right) state. Black frames indicate the expected outcome for an ideal fan-out circuit. (b) Measured (gray bars) and ideal (black frame) expectation values of the multiqubit Pauli operators $\hat{O}$ of the output state with non-zero ideal values when the input is prepared in the $|1\rangle$ (left) and $|+\rangle$ (right) state. The top and bottom of the red-shaded area indicate the maximum and minimum of the measured expectation values of the rest of the Pauli operators whose ideal value is zero. (c) Extracted output state fidelity (orange circles) and the expectation values of the joint- X operators of the output qubits (blue triangles) for input states parameterized by the polar angle θ (fixing the azimuthal angle $\phi = 0$) and ϕ (fixing $\theta = \pi/2$). Solid lines indicate the average output-state fidelity (orange) and fits to a sinusoidal function (blue).

using the equal superposition state $|+\rangle$ as the input and extract an output state fidelity of 0.803, see Fig. 2(a).

In both reconstructed density matrices, we do not observe obvious unexpected off-diagonal elements, suggesting that coherent errors are small. We further verify this by calculating the expectation value of multiqubit Pauli operators from the density matrices. From the four-qubit output states of the input state $|1\rangle$, we extract the measured expectations values of Pauli operators with nonzero ideal values and observe measured values on average 0.76(7) times their ideal value of ± 1 [see Fig 2(b)]. In contrast, the measured expectation values that ideally vanish remain between ± 0.05 . We observe the same fractional errors for the $|+\rangle$ input state.

To characterize our 1-to-4 fan-out gate acting on arbitrary input states, we prepare Q^{in} in a family of superposition states $|\psi_{\text{in}}\rangle = \cos(\theta/2)|0\rangle + e^{i\phi} \sin(\theta/2)|1\rangle$ parametrized by the polar angle θ and the azimuthal angle ϕ . For each prepared state, we characterize the corresponding output state using quantum state tomography. First, we sweep the polar angle θ while fixing the azimuthal angle $\phi = 0$, essentially varying the excitation probability in the superposition state. We find an average fidelity of 0.79(2), see Fig. 2(c) (orange). As varying θ changes the X parity of the output state, we calculate $\langle X_1^b X_2^b X_3^b X_3^c \rangle$ from the reconstructed density matrices (blue) and observe that it follows a sinusoidal oscillation in the expectation value of the joint- X operator as expected for the ideal state. We fit the contrast of the sine oscillation to 0.730(6), with the ideal value being 1. The measured contrast being 92% of the average fidelity is a consequence of dephasing errors and midcircuit readout errors, which affect the joint- X operator more strongly than the fidelity. Similarly, we fix the polar angle $\theta = \pi/2$ and sweep the azimuthal angle ϕ , varying the phase of an equal superposition state. The sweep gives an average fidelity of 0.78(1) and a joint- X operator oscillation contrast of 0.736(4). As observed, the fidelity is primarily independent of the input state. This suggests that the feedforward-based fan-out sequence, which we have realized performs uniformly well for arbitrary input states and has no prominent coherent errors.

IV. ERROR SCALING WITH THE OUTPUT QUBIT NUMBER

We study the scaling of the output-state error $\varepsilon = 1 - F$ with the number n of output qubits. We prepare the input state in the six cardinal states $|0/1\rangle, |\pm\rangle, |\pm i\rangle$ and extract an average error of 0.09(1), 0.14(1), 0.20(2) for $n = 2, 3$, and 4, respectively. We compare the measured errors with a success probability model that considers CNOT gate errors, readout errors, and idling errors, assuming that the errors are uncorrelated, see Appendix C. We find the errors predicted by the error model and from measurement differ by a maximum of 0.014, suggesting quantitative agreement

between the model and the experiment, see Fig. 3(a). We decompose the measured error into its identifiable sources, see Fig. 3(b). For the 1-to-4 fan-out gate, we find CNOT gates, idling, and readout contribute an error of 0.10, 0.07, and 0.03 to the output state.

To investigate the limit of the expected fan-out gate performance independent of the feedforward latency, we run a constant-depth fan-out sequence with Pauli-frame update [28]. To do so, we read out the output qubits when we perform the midcircuit measurement and update

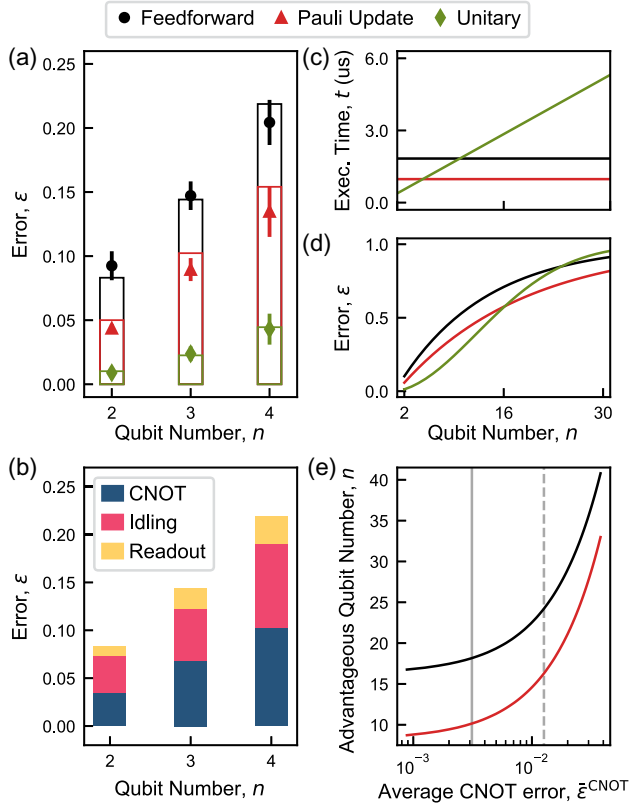


FIG. 3. (a) Fan-out gate error ϵ vs output qubit number n with feedforward control (black circles), Pauli-frame update in postprocessing (red triangles), and the unitary gate sequence (green diamonds). Error bars show the standard deviation over the errors measured from the six cardinal input states. Wireframes of the same color show the expected error derived from a success-probability model, taking into account individual CNOT gate errors, readout errors, and idling errors. (b) Decomposition of the error of the feedforward fan-out gate into CNOT gate errors (blue), idling errors (pink), and readout errors (yellow). (c) Circuit execution time of the three implementations. (d) Expected error calculated using the success probability model described in the main text. (e) Number of qubits n , above which the feedforward (black) and Pauli-frame update (red) implementation show an advantage over the unitary circuit as a function of the average CNOT gate error $\bar{\epsilon}^{\text{CNOT}}$. The vertical dashed line shows $\bar{\epsilon}^{\text{CNOT}}$ of the device used for this experiment. The vertical solid line marks the average idling error for an idle period of a CNOT gate time $\bar{\epsilon}^{\text{idling}}$ on this device.

the Pauli reference frame in postprocessing. In this scenario, we avoid the contribution to the total error stemming from qubit idling during the feedforward part of the sequence, while all other error sources remain. For the two-, three-, and four-qubit output states, we obtain an average error of 0.044(3), 0.09(1), and 0.14(2) over the six cardinal input states. For comparison, we calculate the error expected from the success probability model, excluding the idling error introduced during the feedforward latency, and observe quantitative agreement between the measured and expected error. Our success probability model being verified by both the feedforward and the Pauli-frame update data supports our assumption that the errors from different sources are uncorrelated and also allows us to analyze the ideal case in which the latency from the electronics is negligible.

For reference, we run a static, unitary fan-out circuit between nearest-neighbor qubits, see Appendix B, and compare its performance with the constant-depth (i.e., feedforward and Pauli-frame update) protocols. At two to four output qubits, the executed unitary circuits show smaller errors than the equivalent constant-depth circuits, see Fig. 3(a). This is expected from the shallower circuit depth, fewer gates, and the smaller number of qubits in the unitary protocol.

However, we expect the constant-depth circuits to perform better with a larger number of output qubits. Indeed, the execution time increases linearly with the output qubit number n in the case of the unitary circuit, while it remains fixed for the constant-depth circuit, see Fig. 3(c). The different scaling of the execution time causes the idling error to scale quadratically for the unitary circuit and linearly for the constant-depth circuits, see Appendix C, which leads to the benefit of the constant-depth circuit at large output qubit numbers. We calculate the expected output-state error of the implemented protocols with our success probability model. We find that the feedforward implementation is expected to outperform the unitary implementation when the fan-out is applied to 25 or more output qubits, while the Pauli frame update implementation shows an advantage over the unitary circuit for 17 output qubits or more, see Fig. 3(d).

The constant-depth implementations utilize more CNOT gates than the unitary implementation. Thus, we expect the constant-depth circuits to be advantageous at lower qubit numbers when the CNOT gate error is lower. With the other errors unchanged, we vary the average CNOT gate error $\bar{\epsilon}^{\text{CNOT}}$ and predict when the constant-depth implementations outperform the unitary circuit, see Fig. 3(e). $\bar{\epsilon}^{\text{CNOT}}$ is lower bounded by the idling error for an idle period of the CNOT gate time $\bar{\epsilon}^{\text{idling}}$. At the limit where $\bar{\epsilon}^{\text{CNOT}}$ approaches $\bar{\epsilon}^{\text{idling}}$, the feedforward implementation is advantageous beyond 19 qubits, and the Pauli-frame update implementation is advantageous beyond 11 qubits.

V. DISCUSSION AND OUTLOOK

In this work, we present a prototypical 1-to-4 fan-out gate with real-time signal processing and feedforward control. We characterize the output states with quantum state tomography and extract an average fidelity of 0.79(2) and 0.78(1) for the input states parameterized over the polar and azimuthal angles. We study the scaling of the output-state error, which we decompose into individually characterized error sources, with the output qubit number. Compared with the unitary circuit, the constant-depth protocol is expected to yield a benefit at 25 output qubits with the real-time feedforward control realized in this experiment or at 17 output qubits in the limit at which the feedforward delay is negligible.

Our work shows that the performance of a fan-out gate on a linear nearest-neighbor qubit array can be optimized by reducing the circuit depth with adaptive circuits. Further improvements could be made by reducing the sequence length through faster quantum or classical operations, increasing the qubit coherence, and investigating efficient dynamical decoupling sequences beyond CPMG pulses during the idling time. We emphasize that we implement the circuit with real-time feedforward control, which allows the output state to be used for further processing in more complex protocols, such as the quantum Fourier transform [18] or Shor's algorithm on a nearest-neighbor connected lattice of qubits [14]. It can also find applications in protocols requiring nonlocal entanglement, for example, quantum low-density parity check (LDPC) codes [29].

We note that in parallel to our work, another constant-depth quantum fan-out gate was demonstrated on superconducting circuits with up to 50 output qubits with Pauli-frame update [30]. The experiment observes a crossover at seven qubits, above which the constant-depth circuit outperforms the unitary circuit. We find the result similar to our work. The two works complement each other, as Ref. [30] experimentally explores an output size at which the constant-depth circuit outperforms the unitary sequence, while we implement the real-time feedforward recovery pulses required for using the output states in a quantum algorithm and study the error composition. We compare our work with recent constant-depth quantum fan-out gate experiments in Appendix E.

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J.-C.B. and Y.S. conceived the project. Y.S. acquired the data. J.-C.B. and Y.S. contributed to the analysis. C.H., L.B., and Y.S. contributed to the classical feedforward development. I.B., M.K., and M.P. contributed to the measurement setups. A.F. and D.C.Z. fabricated the device designed by F.S.. A.W. and J.-C.B. supervised the project. J.-C.B. and Y.S. wrote the manuscript with inputs from all authors.

DATA AVAILABILITY

The data that support the findings of this article are openly available [31].

APPENDIX A: SAMPLE AND EXPERIMENTAL SETUP

We perform the experiment on the 17-qubit superconducting quantum processor shown in Fig. 4. The transmon islands, coplanar waveguides, and couplers are patterned with photolithography and reactive-ion etching into a 150-nm niobium thin film sputtered onto a high-resistivity silicon substrate. Aluminium-titanium-aluminium trilayer airbridges connect the otherwise separated ground planes. We fabricate the aluminium-based Josephson junctions of the transmon qubits using electron-beam lithography (EBL) and shadow evaporation.

We characterize the coherence property of each qubit with standard methods [32], see Fig. 5. We extract a median relaxation time $T_1 = 46 \mu\text{s}$, dephasing time $T_2^* = 28 \mu\text{s}$, and Hahn-echo dephasing time $T_2^{\text{echo}} = 48 \mu\text{s}$.

In the experiment, we implement single-qubit gates with 32-ns microwave DRAG pulses [21] with Gaussian envelopes truncated at $\pm 2.5\sigma$, where $\sigma = 6.4 \text{ ns}$. The CZ gates are realized with net-zero flux pulses [23,33] with an average duration of 104 ns. We add 20-ns buffers before and after each flux pulse to account for the finite size of the predistortion filters [34] and round each total CZ gate time to an integer multiple of 8 ns to be commensurate with the granularity of the waveform playback of the control instruments. This results in an average total duration of the CZ gate of 144 ns.

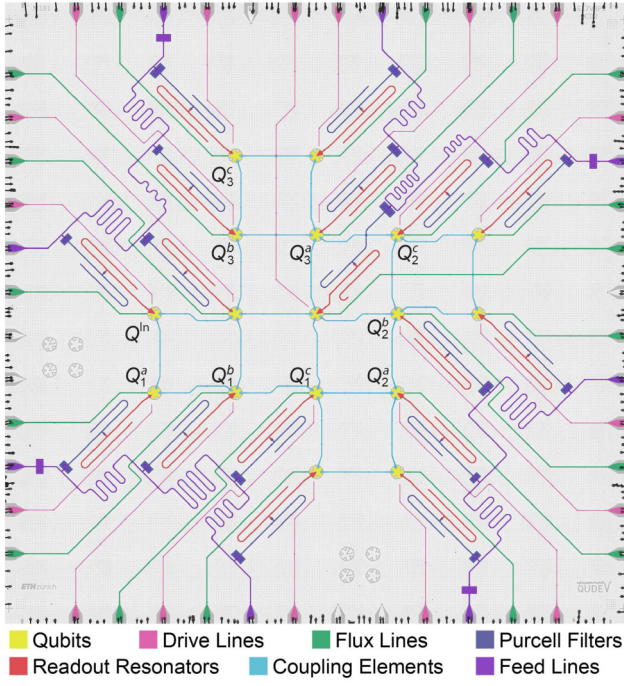


FIG. 4. False-color micrograph of the device used for the experiment. The qubits involved in the fan-out gate are labeled in the figure.

We benchmark the performance of the single-qubit gates with randomized benchmarking [35,36] and the performance of two-qubit gates with interleaved randomized benchmarking [37–39], see Fig. 5. We find a median single-qubit error $\varepsilon_{1Q} = 0.05\%$ and two-qubit error $\varepsilon_{2Q} = 1.1\%$. We characterize the single-shot readout performance by preparing the qubits in either computational basis state $|0\rangle$ and $|1\rangle$ and determining the readout assignment probability matrix with single-shot readout. To initialize our qubit register, we perform a qubit readout before the start

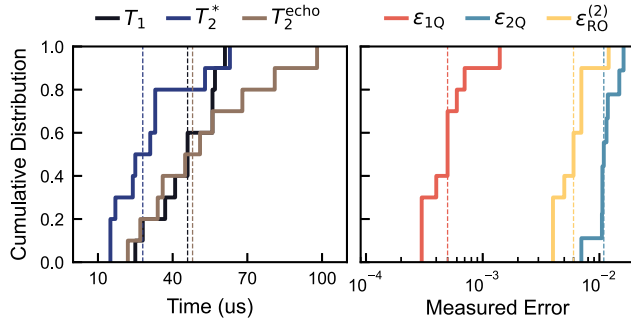


FIG. 5. Cumulative distributions (integrated histograms) of (left panel) qubit relaxation time T_1 (black), dephasing time T_2^* (blue), and Hahn-echo dephasing time T_2^{echo} (brown); (right panel) single-qubit gate (red), simultaneous two-qubit gate (cyan), and two-state readout (yellow) errors. Vertical dashed lines indicate the median values of the corresponding quantity.

of the gate sequence and reject all instances where qubits are found in the excited state. The readout error $\varepsilon_{\text{RO}}^{(2)}$ is calculated as the average of the misassignment probability $P_{0|1}$ and $P_{1|0}$, where $P_{a|b}$ stands for the probability of reading out the qubit in state a when preparing in state b . We find a median readout error $\varepsilon_{\text{RO}}^{(2)} = 0.6\%$.

The 17-qubit device is installed at the 10-mK temperature stage of a dilution refrigerator in a standard wiring and shielding configuration [40]. We connect the room-temperature electronics to the device with signal lines comprising microwave components and coaxial cables, see Fig. 6. The dc source provides a constant bias current for each qubit to set its idle operation frequency. The arbitrary waveform generators (HDAWG) generate voltage pulses at a rate of 2.0 GSa/s to implement two-qubit gates. The dc and IF signals are combined with bias tees at room temperature. We use super-high-frequency qubit controllers (SHFQC) to drive and read out the qubits. The SHFQC drive channels generate drive pulses at the qubit-transition

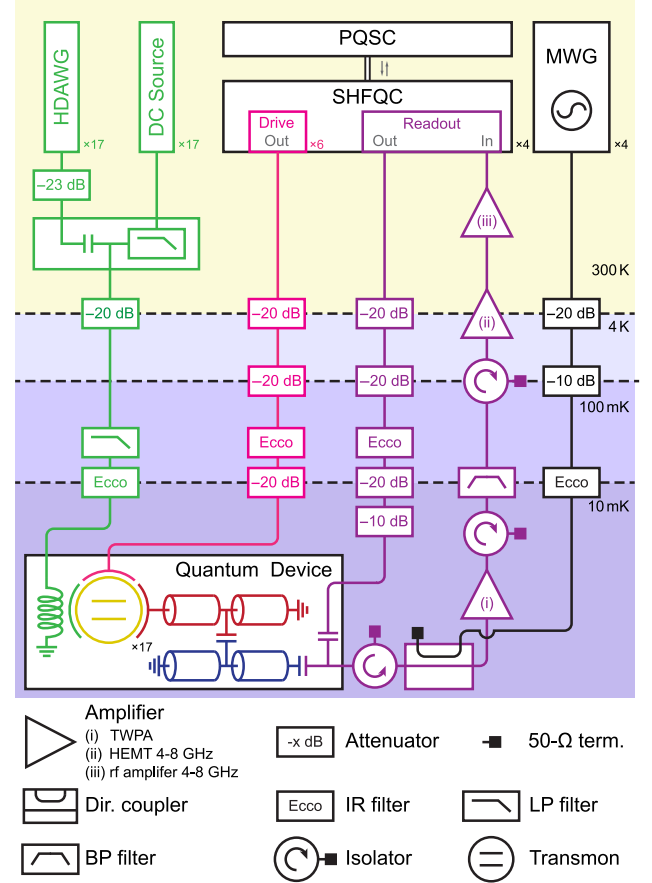


FIG. 6. Schematic diagram of the experimental setup. Flux lines (green), drive lines (pink), and readout lines (purple) transmit the signal between the control electronics and the device, including transmon qubits (yellow), readout resonators (red), and Purcell filters (blue). The background colors indicate the temperature stages of the experimental setup.

frequencies with a double frequency conversion scheme [41]. The SHFQC readout output channel generates multiplexed readout tones at the readout resonator frequencies, which after interacting with the device pass through an amplification chain consisting of a wide-bandwidth near-quantum limited traveling-wave parametric amplifier (TWPA) [42], a high-electron-mobility transistor (HEMT) amplifier, and a low-noise, room-temperature amplifier. The amplified signal is digitized and integrated for 400 ns by the SHFQC readout input channel. After the mid-circuit measurement, the integration result is compared to a predefined threshold to discriminate the projected state of a qubit, and all thresholded results are forwarded to a programmable quantum system controller (PQSC) to be interpreted with look-up tables (LUTs) as indices referring to the feedforward control pulses. The indices are subsequently sent to the SHFQC drive channels, which play the recovery pulses. The feedforward idling time is 800 ns, including the signal propagation delay, the classical processing time, and a 40-ns buffer time. This control electronics architecture allows for a straightforward extension to a 60-qubit setup while maintaining the same feedforward idling time.

When implementing the feedforward logic with LUTs, the PQSC allows for the processing of up to 16 binary mid-circuit readout results, which limits the fan-out output state to nine qubits. For processing the logic for larger output qubit numbers, one could use logical circuits programmed with an FPGA [43]. Following Eq. (1), feedforward control indices can be obtained by applying adders to subsets of the midcircuit readout results. Modern FPGAs typically contain digital signal processing (DSP) slices as a dedicated hardware resource optimized for arithmetic operations. For this experiment, each DSP slice can be configured to perform an accumulative addition over a subset of midcircuit measurement outcomes and generate the feedforward control bit for an output qubit. With an off-the-shelf FPGA, one can process the feedforward logic of our constant-depth fan-out circuit for $O(10^3)$ output qubits or more.

APPENDIX B: GATE SEQUENCE AND TIME BUDGET

We map the gate sequence in Sec. II to ten qubits selected from the 17-qubit quantum device, see Fig. 7. The mapping allows for the execution of every parallel two-qubit gate step without noninteracting qubits crossing each other in frequency. Adjusting the output qubit number could be achieved by adding or removing groups of three qubits at the input qubit end.

We realize the 1-to-4 constant-depth fan-out circuit with the native gate set in our architecture, see Fig. 8. We implement single-qubit x and y rotations with 32-ns DRAG pulses [21]. We realize single-qubit z rotations with virtual

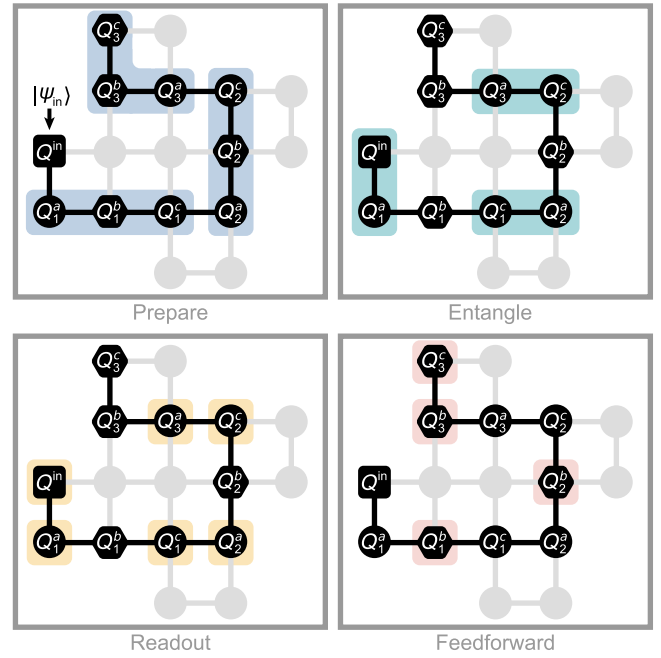


FIG. 7. Mapping of a 1-to-4 fan-out gate onto a 17-qubit superconducting quantum device. Qubits involved in the algorithm are highlighted in black. Q^{in} (square) carries the input state $|\psi_{\text{in}}\rangle$. In each step, qubits being driven or read out are highlighted with a background color. The protocol maps the four-qubit output state onto Q_1^a, Q_2^b, Q_3^c , and Q_4^d (hexagons).

Z gates [22], with the exception of the feedforward Z gate being decomposed into physical x and y rotations $R_x(\pi/2)R_y(\pi)R_x(-\pi/2)$. Further upgrades of the control software would allow for conditional virtual Z gates and thus reduce this overhead. We decompose CNOT gates into CZ gates [23,33] and single-qubit y rotations. During the feedforward idling time, we apply two CPMG dynamical decoupling pulses on every output qubit to mitigate low-frequency noise.

With the aforementioned decomposition, the prepare, entangle, measurement, and feedforward step take 352, 208, 400, and 928 ns, respectively. The whole sequence lasts 1888 ns, with 49% of the time required for the feedforward control. Comparably, the unitary fan-out sequence takes 560 ns due to a shorter circuit depth, see Fig. 8(b).

The 928-ns feedforward time budget consists of 670-ns classical processing delay in the control electronics, 85-ns signal propagation delay between the electronics and the quantum processor, 128-ns feedforward control pulse, and 45-ns buffer time. The largest fraction of the latency is due to constraints of the commercial control electronics with fixed signal-processing pipeline and timing. To achieve a shorter processing time, one could develop custom FPGA code [3,44] and optimize the process flow for the application. With an off-the-shelf FPGA, feedback latency as low as 150 ns is achievable [3,19]. This processing time is significantly shorter than the qubit

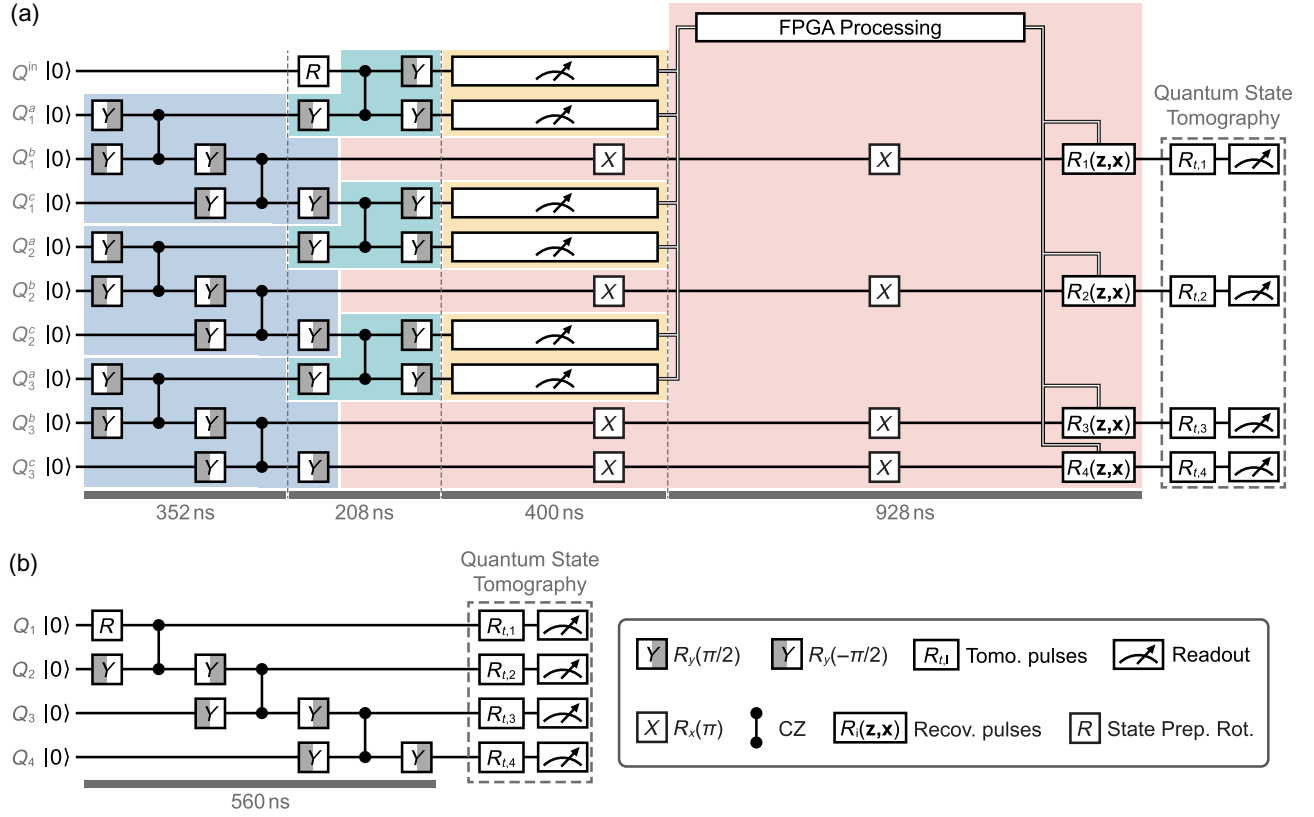


FIG. 8. (a) Decomposing the 1-to-4 fan-out gate sequence with single-qubit rotations and CZ gates. The time budget for each step is shown at the bottom of the figure. Background colors correspond to the prepare (blue), entangle (cyan), measure (yellow), and feedforward (red) steps depicted in Fig. 1. (b) Gate sequence of a unitary 1-to-4 fan-out gate.

coherence time of state-of-the-art superconducting quantum processors and is beneficial for achieving high-fidelity feedforward-empowered circuits. Further reduction in the latency could be achieved by realizing the feedforward logic in application-specific integrated circuit (ASICs), which typically have faster clock rates than FPGAs.

Beyond improvements in electronic design, latency can also be reduced by locating the classical control electronics closer to the quantum device. For example, Ref. [45] demonstrated a round-trip signal propagation delay of just 28 ns by incorporating side-access ports on the dilution refrigerator and minimizing the length of the cryogenic signal lines. Moreover, advances in cryogenic FPGA technology [46,47] offer the potential for further reducing the latency by enabling the feedforward logic processing and pulse generation inside the dilution refrigerator.

We observe that the application of the CPMG dynamical decoupling sequence effectively reduces the error introduced due to decoherence during the feedforward idling time by mitigating the uncorrelated low-frequency noise. It is possible to further decouple noise from the entangled output state by tailoring the dynamical decoupling sequence based on the specific characteristics of the noise present in the system [48]. Besides mitigating noise from idling time, dynamical decoupling techniques can also

improve the performance of quantum gates [49,50] and be integrated into fault-tolerant quantum computing [51]. This ensures a scalable combination between the fan-out sequence and the dynamical decoupling technique.

APPENDIX C: ERROR SCALING OF THE FAN-OUT CIRCUITS

Given the error rate of elementary operations, we theoretically analyze the output-state fidelity of different fan-out sequences based on a success-probability model. First, we assume that the total error of the sequences ε^{tot} is dominated by the individual CNOT gate errors $\{\varepsilon_i^{\text{CNOT}}\}$, measurement errors $\{\varepsilon_j^{\text{meas}}\}$, and idling errors $\{\varepsilon_k^{\text{idle}}\}$. Then, we assume these errors are incoherent and uncorrelated, which yields an independent success rate of each operation of $(1 - \varepsilon)$, where ε is the error rate of the operation. We estimate the success probability of the full sequence by multiplying the success probability of all elementary operations:

$$1 - \varepsilon^{\text{tot}} = \prod_{i=1}^{n_{\text{CNOT}}} (1 - \varepsilon_i^{\text{CNOT}}) \prod_{j=1}^{n_{\text{meas}}} (1 - \varepsilon_j^{\text{meas}}) \prod_{k=1}^{n_{\text{idle}}} (1 - \varepsilon_k^{\text{idle}}), \quad (\text{C1})$$

where n_{idle} , n_{CNOT} , n_{meas} are the number of error-prone operations of that type. We determine $\{\varepsilon_i^{\text{CNOT}}\}$ as the sum of one CZ gate error and two single-qubit errors extracted from randomized benchmarking. We obtain $\{\varepsilon_j^{\text{meas}}\}$ by characterizing single-shot readout (see Appendix A). We model $\{\varepsilon_k^{\text{idle}}\}$ as arising from two independent noise processes during the idling time τ : energy relaxation at rate $1/T_1$ and dephasing at rate $1/T_\phi^{\text{h}}$. Here, $T_\phi^{\text{h}} = [(1/T_2^{\text{echo}}) - (1/2T_1)]^{-1}$ is the dephasing time caused by the high-frequency flux noise not mitigated by the Hahn-echo pulse. The random projection of midcircuit measurement and subsequent feedforward operations Pauli twirls the relaxation and dephasing noise [35,52]. As a result, the residual noise can be described by a Pauli channel:

$$\mathcal{S}(\rho) = (1 - p_X - p_Y - p_Z)\rho + p_X X \rho X + p_Y Y \rho Y + p_Z Z \rho Z, \quad (\text{C2})$$

where

$$p_X = p_Y = \frac{\tau}{4T_1}, \quad p_Z = \frac{\tau}{2T_\phi^{\text{h}}}. \quad (\text{C3})$$

Equation (C1) can be used for predicting the error of the sequences, for which all elementary operations have been benchmarked. To predict the error of a sequence at a circuit size beyond the experiment, we replace individual errors with the average error rate of the same type of error source,

$$1 - \varepsilon^{\text{tot}} = (1 - \bar{\varepsilon}^{\text{CNOT}})^{n_{\text{CNOT}}} (1 - \bar{\varepsilon}^{\text{meas}})^{n_{\text{meas}}} (1 - \bar{\varepsilon}^{\text{idle}})^{n_{\text{idle}}}, \quad (\text{C4})$$

where $\bar{\varepsilon}^{\text{CNOT}}$, $\bar{\varepsilon}^{\text{meas}}$, $\bar{\varepsilon}^{\text{idle}}$ are the average CNOT, measurement, idling errors for the qubits on the device. For brevity, we specify $\bar{\varepsilon}^{\text{idle}}$ as the average idling error for a CNOT gate time t_{CNOT} . Correspondingly, the occurrence n_{idle} is the total idle time of all qubits normalized by t_{CNOT} . We assume that the feedforward latency introduced by classical electronics is μ times t_{CNOT} . In this work, $\mu = 7.5$. We list the occurrence of each error source for the three circuits in Table I.

We note that in the limit of small output qubit number n , ε^{tot} scales quadratically with n for the unitary protocol and linearly with n for the constant-depth protocols (i.e., the feedforward and Pauli frame update implementations).

TABLE I. Occurrences n_{idle} , n_{CNOT} , and n_{meas} of the dominating error sources for the three fan-out circuits discussed in the main text, vs the number of output qubits n .

Circuit	n_{idle}	n_{CNOT}	n_{meas}
Unitary	$(n^2 - 3n + 2)/2$	$n - 1$	0
Feedforward	$n(\mu + 2) - 1$	$3n - 3$	$2n - 2$
Pauli frame update	$2n - 1$	$3n - 3$	$2n - 2$

APPENDIX D: CHARACTERIZATION OF THE OUTPUT QUANTUM STATE

We benchmark the fan-out sequence performance by characterizing the output states with quantum state tomography, see Fig. 8(a). Before each measurement run, we read out every qubit and herald all qubits in the $|0\rangle$ state [53,54]. We estimate the quantum state from a set of positive operator-valued measurements (POVMs), realized by applying single-qubit rotations $R_{t,i} \in \{I, R_x(\pi), R_y(\pi/2), R_y(-\pi/2), R_x(\pi/2), R_x(-\pi/2)\}$ to each qubit before the final readout. To characterize a n -qubit quantum state, we measure in total 6^n combinations. For each combination k , we repeat the measurement and obtain a probability distribution $\mathbf{P}_{Q_1, \dots, Q_n|k} = (p_{0\dots 0|k}, p_{0\dots 1|k}, \dots, p_{1\dots 1|k})$ of projecting the qubits onto each product state of the computational basis. In addition, we characterize the readout assignment probability matrix

$$\mathbf{M}_{Q_i} = \begin{pmatrix} P_{0|0} & P_{1|0} \\ P_{0|1} & P_{1|1} \end{pmatrix} \quad (\text{D1})$$

for each qubit Q_i as described in Appendix A. Assuming uncorrelated readout errors, a readout-error-corrected probability distribution is obtained by applying the inverse of the readout assignment probability matrices to the measured probability distribution [27],

$$\mathbf{P}_{Q_1, \dots, Q_n|k}^{\text{corrected}} = (\mathbf{M}_{Q_1}^{-1} \otimes \dots \otimes \mathbf{M}_{Q_n}^{-1}) \mathbf{P}_{Q_1, \dots, Q_n|k}. \quad (\text{D2})$$

The set of readout-error corrected probability distributions $\{\mathbf{P}_{Q_1, \dots, Q_n|k}^{\text{corrected}}\}$ is used to estimate the density matrix with iterative maximum-likelihood estimation [55]. With the estimated density matrix, we calculate the output-state error ε with respect to the ideal output state.

We verify the convergence of the maximum-likelihood estimation to the output states with a bootstrapping method [56,57]. For each measured tomography dataset, we randomly select subsets of the measurement runs and recombine them into ten bootstrapped datasets. We repeat the tomography analysis discussed above on each bootstrapped dataset and calculate the standard deviation of the extracted errors $\sigma(\varepsilon)$. We average $\sigma(\varepsilon)$ over the six cardinal input states for different fan-out implementations with two, three, and four output qubits, see Table II. We

TABLE II. Mean and variance of the estimated error $\varepsilon \pm \bar{\sigma}(\varepsilon)$ extracted from the bootstrapping tomography analysis for different fan-out implementations and number of output qubits.

Qubit number	Feedforward	Pauli update	Unitary
2	0.092 ± 0.004	0.043 ± 0.003	0.009 ± 0.002
3	0.143 ± 0.002	0.090 ± 0.002	0.024 ± 0.002
4	0.206 ± 0.002	0.132 ± 0.002	0.043 ± 0.002

TABLE III. Comparison of the recent works implementing constant-depth fan-out in superconducting circuits. See text for details of the notations. Fidelities are reported as * truth table fidelity, [†] Monte-Carlo state certification-based estimation, and [‡] output state fidelity.

Ref.	Method	$n_{\max}$	$n_{\text{crossover}}$	$F_{1 \rightarrow 3}$	N	d_{meas}	n_{meas}	d_{CNOT}	n_{CNOT}
Hashim2024 [19]	Feedforward	3	...	0.68*	$2n$	2	$2n - 1$	3	$3n - 2$
Bäumer2024 [30]	Pauli frame update	51	7	0.92 [†]	$2n - 1$	1	$n - 1$	5	$3n - 4$
This work	Feedforward	4	25	0.86 [‡]	$3n - 2$	1	$2n - 2$	3	$3n - 3$

find $\sigma(\varepsilon)$ more than one order of magnitude lower than the measured ε , verifying the convergence of the estimation method.

APPENDIX E: COMPARISON OF RECENT FAN-OUT EXPERIMENTS

In Table III, we compare our work with recent constant-depth quantum fan-out gate experiments [19,30].

Regarding the physical setup and protocol performance, we state the implemented method, the maximal number of output qubits $n_{\max}$, the number of output qubits $n_{\text{crossover}}$ at which the constant-depth circuit outperforms the unitary circuit, and the fidelity of the 1-to-3 fan-out $F_{1 \rightarrow 3}$. Reference [19] and our work realize a deterministic fan-out circuit with real-time feedforward control on quantum hardware. Reference [30] extended the experiment to up to 51 output qubits and experimentally observed an advantage of constant-depth circuits. The reported fidelity varies due to the different evaluation methods and different susceptibility to noise.

In terms of the circuit composition, we compare the total number of required physical qubits N , the depth (number of rounds) of midcircuit measurements d_{meas} , the number of midcircuit measurements n_{meas} , the depth of CNOT gates d_{CNOT} , and the number of CNOT gates n_{CNOT} for a given output qubit number n . The three circuits have a similar number of CNOT gates. Reference [19] and our work require fewer rounds of parallel CNOT gates, while reference [30] consists of fewer midcircuit measurements.

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