

Noise correlations in an atom-based quantum dot array

M.B. Donnelly^{1,2,3,*} J. Rowlands^{1,2,3,*} L. Kranz^{1,2,3} Y.L. Hsueh^{1,2} Y. Chung^{1,2,3}
 A.V. Timofeev^{1,2,3} H. Geng^{1,2,3} P. Singh-Gregory¹ S.K. Gorman^{1,2,3} J.G. Keizer^{1,2,3}
 R. Rahman^{1,2} and M.Y. Simmons^{1,2,3,†}

¹*Silicon Quantum Computing Pty. Ltd., Level 2 Newton Building, UNSW Sydney, NSW 2052, Australia*

²*School of Physics, UNSW Sydney, NSW 2052, Australia*

³*Centre for Quantum Computing and Communication Technology, UNSW Sydney, NSW 2052, Australia*

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Correlated noise across multiqubit architectures is known to be highly detrimental to the operation of error-correcting codes and the long-term feasibility of quantum processors. The recent discovery of spatially dependent correlated noise in multiqubit architectures of superconducting qubits arising from the impact of cosmic radiation and high-energy particles giving rise to quasiparticle poisoning within the substrate has led to intense investigations of mitigation strategies to address this. Correlated noise in semiconductor spin qubits is also now receiving attention, as this platform begins to scale. Here we report the magnitude, frequency, and spatial dependence of noise correlations between four silicon quantum dot pairs as a function of interdot distance at frequencies from 0.3 to 1 mHz. We find the magnitude of charge-noise correlations, quantified by the magnitude square coherence C_{xy} , are significantly suppressed from > 0.5 to < 0.1 as the interdot distance increases from 75 to 300 nm. Using an analytical model we confirm that, in contrast to superconducting qubits, the dominant source of correlated noise arises from low-frequency charge noise from the presence of two level fluctuators (TLFs) at the native silicon-silicon dioxide surface. Knowing this, we conclude with a timely discussion of charge-noise mitigation strategies.

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I. INTRODUCTION

Error correction remains a major challenge in realizing a quantum processor that can perform calculations exponentially faster than classical computers. Quantum error correction requires that not only are errors sufficiently small but that they are uncorrelated [1,2], since errors found to be bunched in either space or time impede error-correction protocols and significantly lower the threshold required for fault tolerance [3,4]. This poses a significant challenge for qubits in the solid state where phonons and electric-field fluctuations in the qubit chip can lead to correlated qubit errors. For superconducting qubits, it has been recently shown that correlated errors can arise from the absorption of background cosmic radiation and high-energy particles within the substrate [5–8]. Such

absorption events produce energetic phonons that break up the paired electrons in the superconducting material, inducing discrete changes in qubit offset charge via quasiparticle poisoning [7,9,10]. These locally generated phonons propagate through the chip and induce spatial correlations in charge noise between qubits, typically observed on the approximately mm length scale [5,7].

Substantial progress has been made in the past few years in another solid-state platform—silicon spin qubits. Here, error rates of single- and two-qubit gates above 99% have been demonstrated in a number of systems including atom-based qubits [11,12] and Si/SiGe qubits [13,14], that if scaled to larger system sizes, are suitable for fault-tolerant operation. For quantum error correction in this material system it is useful to also quantify and identify the source of correlated charge noise. Charge noise can impact semiconductor spin qubits by coupling to voltage pulses used for electrically driven control schemes [15,16], as well as exchange coupling [17,18], which can affect both single- and two-qubit gates. Over the past decade, the magnitude of charge noise in silicon spin qubits primarily due to the presence of low-frequency noise caused by two level fluctuators (TLFs) [19–23] has been systematically lowered by improving the materials quality and thereby mitigating

*These authors contributed equally to the work.

†Contact author: michelle.simmons@unsw.edu.au

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the effect of these TLFs [24,25]. In particular, exceptionally low charge-noise levels ($S_0 = 0.0088 \mu\text{eV}^2/\text{Hz}$) have been observed in epitaxial spin qubits realized using phosphorus atoms embedded in high-quality crystalline silicon [25].

In this work, we experimentally map the magnitude, frequency, and spatial dependence of noise correlations as a function of distance in a linear array of ten phosphorus donor quantum dot pairs with a separation of 75 nm between neighboring quantum dot pairs. Using frequency multiplexed charge readout we perform simultaneous charge-noise measurements on four of the ten dot pairs in the array using the technique of charge transition peak tracking [22,25]. Here we simultaneously track the location in gate space of charge transitions from our charge sensors to several of the dot pairs and quantify noise correlations between them over a 16-h period. Our results confirm a suppression of charge-noise correlations as we increase the intersite separation up to 300 nm. We also show a frequency dependence of the correlations, which shows that they fall with increasing frequency up to

1 mHz, a trend also observed in the Si/SiGe material system [26–28]. We then model the source of the charge-noise correlations observed in our device by simulating charge traps at the native silicon-dioxide surface as TLFs.

II. RESULTS

Charge-noise correlations were measured in a phosphorus-doped silicon (Si:P) quantum dot array [29], one of the largest silicon architectures patterned using STM lithography to date [Figs. 1(a) and 1(b)]. Each pair of phosphorus-doped quantum dots is controlled by an electrostatic gate (G1-G10) and is tunnel coupled to a reservoir (R1-R10) with each reservoir connected to a dedicated resonant tank circuit on a separate chip [Fig. 1(c)]. All ten tank circuits (consisting of superconducting thin-film NbTiN spiral inductors) are connected via a common rf transmission line allowing for simultaneous frequency multiplexed readout of all quantum dot pairs.

To assess the spatially dependent noise correlations in this device we considered four of the quantum dot pairs

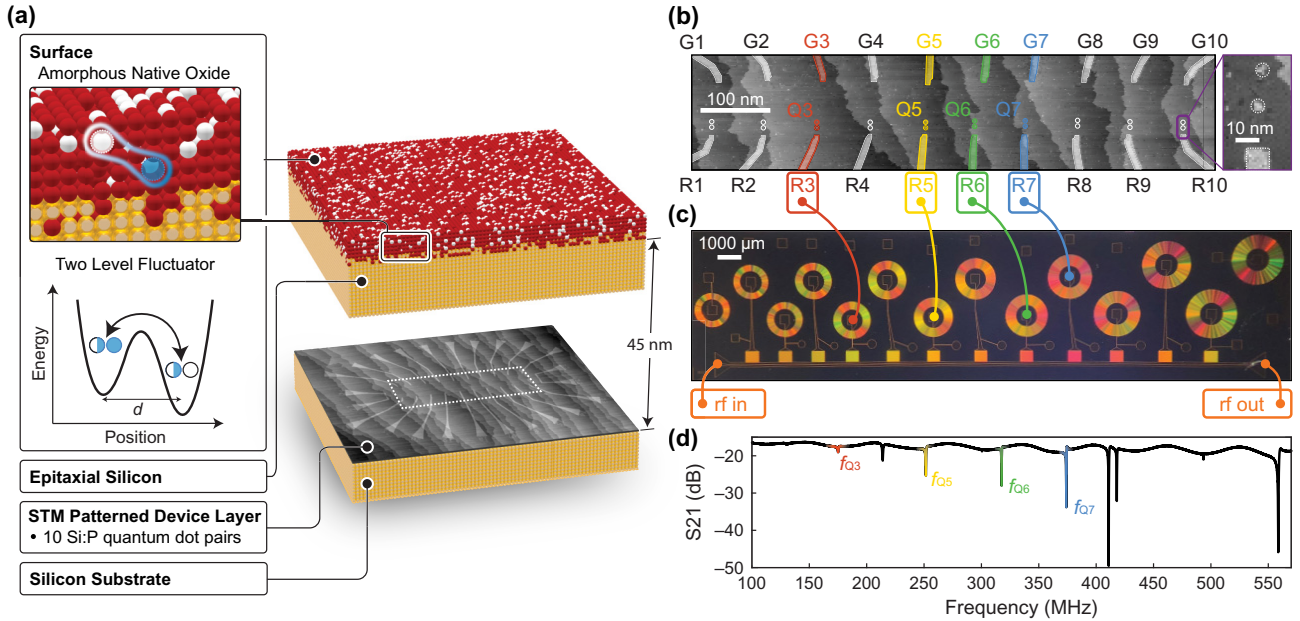


FIG. 1. Noise correlations in a multiplexed quantum dot array in silicon. (a) A diagram of the device material stack showing (from bottom to top), the silicon substrate, on which 10 Si:P quantum dot pairs containing approximately two phosphorus atoms are patterned using STM lithography [see (b)]. The quantum dot pairs are encapsulated with 45 nm of epitaxial silicon, which is terminated with an amorphous native silicon dioxide surface. Pairs of charge traps in the oxide form two level fluctuators (box, left), where electrons tunnel back and forth between the charge traps. This tunneling forms a flip-flopping dipole $p = ed/2$, where d is the separation between the traps, introducing correlated charge noise on the quantum dot pairs. (b) STM image of the array showing a linear set of ten pairs of quantum dots, each connected to a reservoir (R1-R10) and controlled by a gate (G1-G10). Four of the quantum dot pairs were studied in this work, marked Q3, Q5, Q6, and Q7, measuring charge-noise PSD and correlations over interqubit separations from 75 up to 300 nm. An STM image of a single Si:P quantum dot pair (Q10) is shown in the inset to the right showing two approximately 2P dots separated by 11.4 nm, with the lower dot 13.5 nm away from the reservoir. (c) Each quantum dot pair reservoir is connected with a bond wire to an rf multiplexing chip containing NbTiN spiral inductors. Each inductor forms a separate LC resonant circuit for performing charge readout on each qubit individually. Simultaneous charge readout on multiple qubits is performed using frequency multiplexing through the single common rf transmission line (rf_{in}, rf_{out}). (d) Frequency dependence of the S21 parameter of the multiplexing chip in transmission, with the relevant resonances for readout marked f_{Q3} , f_{Q5} , f_{Q6} , f_{Q7} .

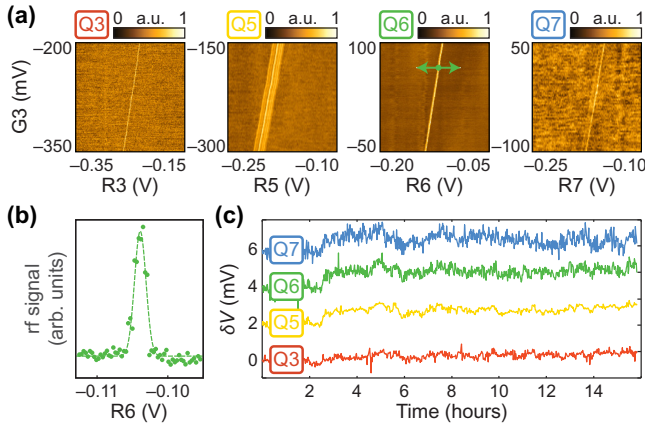


FIG. 2. Frequency multiplexed readout of four quantum dot pairs Q3, Q5, Q6, and Q7. (a) Measurements of the multiplexing chip rf response as the gate (G) and reservoir (R) voltages are swept for Q3, Q5, Q6, and Q7. The bright charge transition peaks running almost vertically indicate the loading of an electron from the reservoir onto the first dot, and are tracked over time to determine charge-noise levels in the device. The doubling of the transition peak in Q7 is the result of tunneling from the top quantum dot to the reservoir [29], and the raised background signal in Q5 likely due to an unintended resonance in the rf circuit. (b) The rf response (circles) at the transition peak for Q6 [marked by arrows in (a)] with a Gaussian fit (dotted line). The Gaussian fit is used to find the center of the charge-transition peak in voltage space. (c) Simultaneous time traces of the location in voltage space of the reservoir to the bottom dot charge transition for Q3, Q5, Q6, and Q7, with each data point taking 72 s to measure and the entire trace measured over approximately 16 h.

in the device, marked Q3, Q5, Q6, and Q7 as shown in Fig. 1(b) (see the Appendix for a summary of the key parameters for all ten quantum dot pairs.). In Fig. 1(d) we show the resonant frequency trace of the rf transmission line where the resonant frequencies of the tank circuits connected to Q3, Q5, Q6, and Q7 are highlighted. We perform dispersive charge readout by probing the response of the rf transmission line at the resonant frequency of each tank circuit as we sweep the voltage applied to the reservoir (R) and gate (G). When an electron tunnels between the reservoir and the lower quantum dot it induces a shift in the rf response, which can be used to map out the charge-stability diagrams for each quantum dot pair, as shown in Fig. 2(a). To obtain the charge-noise spectrum for each of the dot pairs we track the location of the reservoir to the bottom dot charge transition for Q3, Q5, Q6, and Q7 simultaneously in the charge-stability diagram over a period of approximately 16 h [25]. The center of the charge transition is obtained by fitting a Gaussian function to the peak in the rf signal [Fig. 2(b)] with a single-peak trace taking 72 s. The measured peak positions of the four transitions Q3, Q5, Q6, and Q7 over the approximately 16-h measurement are plotted in Fig. 2(c). From these time traces

we calculated the charge-noise power spectral density and interdot correlations.

We first investigate the noise properties of each site individually by analyzing the experimental time traces in Fig. 2(c) and calculate the power spectral density (PSD), shown in Fig. 3(a). We observe that the PSD of charge noise $S(f)$ follows a power-law dependence $S(f) = S_{1\text{ mHz}}/(f \times 10^{-3})^\alpha$ where $S_{1\text{ mHz}}$ corresponds to the PSD value at 1 mHz, and α determines the slope of $S(f)$ in frequency. Due to the focus on the low-frequency range of our experiment we compare the PSD amplitude at 1 mHz $S_{1\text{ mHz}}$, within the bandwidth of our experiment. White noise is observed at frequencies > 2 mHz (gray shaded regions), where the device noise becomes lower than the experimental noise floor. The power-law nature of the low-frequency charge noise has been observed previously in semiconductor qubit platforms and attributed to the presence of an ensemble of TLFs; either formed at the surface, at dielectric interfaces, or within nearby oxides [15,19,20,22,24,25,30]. Due to their crystalline environment, donor devices have been shown to exhibit extremely low levels of charge noise since they are well separated from the surface TLFs by a protective layer of epitaxial silicon [25,30]. For the four quantum dot pairs measured in this device (see methods) we measure the PSD amplitude at 1 mHz $S_{1\text{ mHz}}$ with a range between 4.6×10^{-9} eV²/Hz and 10.6×10^{-9} eV²/Hz. For the spectral exponent, we extract values in a range between 1.0 and 1.6. These values for $S_{1\text{ mHz}}$ and α are consistent with previously reported values for donor devices [18,25,31].

To understand the nature and impact of the potential sources of noise in our devices we explicitly performed simulations of charge noise originating from TLFs located at the Si/SiO₂ native oxide surface located 45 nm above the device. To model the switching noise of TLFs we created an analytical model [illustrated in Fig. 3(b), top] based on the standard tunneling model of TLFs [32,33]. We populate an oxide layer (1100 nm $\times$ 1100 nm $\times$ 2 nm) with charge traps separated by an average distance of 15 nm as determined in previous native oxide surfaces by Shamim *et al.* [30]. This results in a total of 5378 charge traps populating the oxide interface. We consider that each trap consists of a positive charge $+e$ (where e is the elementary charge of an electron), such that when pairs are formed between nearest-neighbor traps they form a double-well potential as shown in Fig. 1(a). Each pair shares two electrons so that the system remains charge neutral. The first electron in the pair gives a negative charge $-e$ bound by the two $+e$ traps giving a net charge of $e/2$ on each trap. When the second electron occupies only one of the traps, the trap pair becomes a dipole with a net charge $-e/2$ on the occupied trap and $+e/2$ on the unoccupied trap. As the second electron tunnels between the traps the dipole flip flops creating a time-dependent potential with dipole moment $p = \pm ed/2$ where d is the distance between the

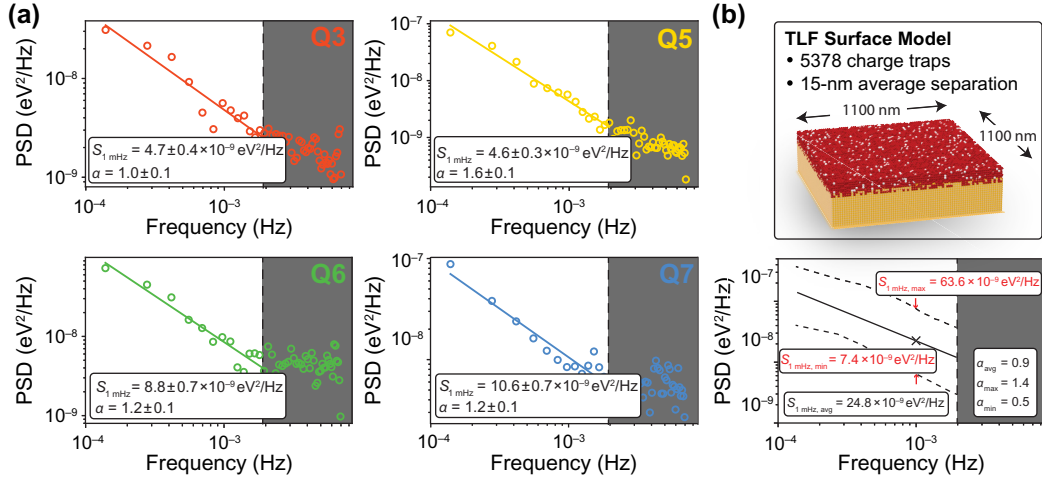


FIG. 3. Power spectral density of quantum dot pairs Q3, Q5, Q6, and Q7. (a) Measurements of the PSD for four quantum dot pairs in our array Q3, Q5, Q6, and Q7 (colored circles) with fits to the data (solid line) used to extract the $S_{1\text{ mHz}}$ and α parameters and uncertainties, before the onset of white noise at frequencies greater than 2 mHz. The onset of white noise is indicated by the gray shaded region. (b) (Top) An illustration of the theoretical model used to simulate charge noise in the silicon quantum dot array. The surface oxide is populated with 5378 TLFs separated by an average distance of 15 nm to model the charge traps that occur at the native oxide surface. (Bottom) Calculations of the PSD from the modeled time-dependent potentials $V(t)$ evaluated at over 500 points in the quantum dot plane. The average PSD over the > 500 points is shown by the black line, and the range shown by the dashed lines. The average modeled PSD amplitude at 1 mHz is $S_{1\text{ mHz}} = 24.8 \times 10^{-9} \text{ eV}^2/\text{Hz}$ (black cross) with a range between $7.4 \times 10^{-9} \text{ eV}^2/\text{Hz}$ and $63.6 \times 10^{-9} \text{ eV}^2/\text{Hz}$ (red arrows). The average modeled spectral exponent is $\alpha = 0.9$ with a range between 0.5 and 1.4.

traps. This flip-flopping dipole generates a random telegraph signal (RTS) with a distribution given by $e^{-f_c t}$ where the center frequency $f_c = f_0 e^{-2\alpha_T d}$. Here f_0 represents the attempt frequency, typically on the order of $f_0 \sim 10^{12}$ Hz in solids [30] and $\alpha_T = \sqrt{2m^* \phi_B / \hbar^2}$, where $\phi_B = 0.1$ eV is the conduction-band offset for the native oxide trap states at the Si-SiO₂ interface [30] and m^* is the electron effective mass. To generate the RTS in our model, we determine whether the dipole is flipping or not after a time interval dt by picking a random number between 0 and 1, if the random number is higher than $e^{-f_c dt}$ then the dipole flips, otherwise the dipole remains the same. The fluctuating potentials from each flip-flopping dipole are then summed and evaluated at a depth of 45 nm below the oxide layer at each quantum dot position according to $V(r) = \frac{1}{4\pi\epsilon_{\text{Si}}} \frac{p \cdot r}{r^3}$, where $\epsilon_{\text{Si}} = 11.7\epsilon_0$ is the silicon dielectric constant, ϵ_0 is the vacuum permittivity, and r is the vector joining the dipole center and the quantum dot location. The time-dependent potential sum $V(t)$ can then be compared directly to the peak position traces in Fig. 2(c) measured on the device. We evaluated the modeled time-dependent potential $V(t)$ at over approximately 500 points evenly spaced over a 2D grid in the quantum dot layer with dimensions 300 nm by 300 nm. At each point, we calculate the PSD of the modeled time-dependent potential $V(t)$, and in Fig. 3(b) (bottom) we plot the average PSD in the simulated device (black line). Here the dashed lines represent the variation in the PSDs across the device locations in the simulation with a average modeled PSD amplitude at 1

mHz of $S_{1\text{ mHz}} = 24.8 \times 10^{-9} \text{ eV}^2/\text{Hz}$ and a range between $7.4 \times 10^{-9} \text{ eV}^2/\text{Hz}$ and $63.6 \times 10^{-9} \text{ eV}^2/\text{Hz}$. Likewise, the average modeled spectral exponent is $\alpha = 0.9$ with a range between 0.5 and 1.4. The ranges of the modeled values of $S_{1\text{ mHz}}$ and α overlap with our experimental values and are in agreement with previously reported values in Si:P [18,25,31].

We now turn to quantify the spatial dependence of charge-noise correlations affecting the quantum dot pairs in the array. We use the magnitude-squared coherence function $C_{xy}(f)$, widely used in signal processing [34,35] to quantify the correlations between two time-dependent signals $x(t)$ and $y(t)$:

$$C_{xy}(f) = \frac{|S_{xy}(f)|^2}{S_{xx}(f)S_{yy}(f)}, \quad (1)$$

where S_{xx} is the PSD of $x(t)$, S_{yy} is the PSD of $y(t)$, and S_{xy} is the cross-correlation PSD (cross-PSD) between $x(t)$ and $y(t)$. The magnitude-squared coherence C_{xy} takes values between $C_{xy} = 0$ (no correlation) and $C_{xy} = 1$ (fully correlated) for the frequency components of $x(t)$ and $y(t)$. To measure the spatial dependence of the noise correlations we consider pairs of sites according to the physical distance between them: Q5-Q6 and Q6-Q7 are separated by 75 nm, Q3-Q5 and Q5-Q7 by 150 nm, Q3-Q6 by 225 nm and Q3-Q7 by 300 nm. In Fig. 4 we plot C_{xy} of the site pairs (taking the average of the two pairs of sites at separations of 75 and 150 nm) for three different frequencies (0.3,

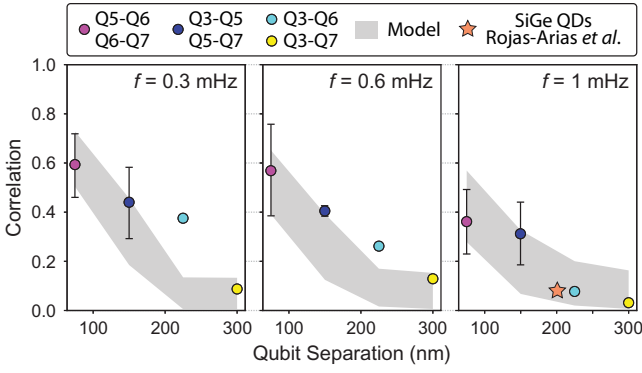


FIG. 4. Frequency dependence of spatial charge-noise correlations. Measurements and simulations of the spatial charge-noise correlations at frequencies of 0.3, 0.6, and 1 mHz. The colored markers indicate correlations calculated using the experimental time traces. Two groups of quantum dot pairs we consider in our device are separated by 75 and 150 nm, and here we plot the average correlation value and use the difference to generate the error bars. The gray shaded region represents the average $\pm\sigma$ for 500 time traces generated using our model. At all frequencies we observe that correlations decrease with increasing separation. At 1 mHz we include data (orange star) from recent work in SiGe quantum dots [28].

0.6, and 1.0 mHz) spanning the accessible frequency range in our experiment. We used both experimentally measured time traces (shown by the colored circles) and time traces generated from our analytical model (gray band). The correlation calculations from our theoretical model average the correlations over 500 time traces using the same trap distribution used in calculating the PSD. The gray regions in Fig. 4 represent the average of these 500 traces $\pm\sigma$. We observe that at 0.3 mHz the modeled charge noise is highly correlated (0.5–0.7) between the site pairs separated by 75 nm as confirmed experimentally where $C_{xy} = 0.6$ was measured. At 0.3 mHz the correlations drop to 0.1 as the separation increases to 300 nm in both our modeling and experimental measurements. Here quantum dot pairs are less likely to be affected by the same TLFs as we increase the interdot distance. At higher frequencies (0.6 and 1 mHz) we see a similar pattern where correlations fall as we increase the site separation. The correlations are, however, consistently smaller across all separations at the higher frequency of 1 mHz compared to 0.3 mHz. This frequency dependence of noise correlations is consistent with recent studies in semiconductor quantum dots [26,28], where further work is needed to explore the relation between this frequency dependence and the microscopic origins of correlated noise.

The results of our model are in agreement with our experimental data, capturing both the falling correlations with site separation and smaller correlations at higher frequencies. This provides evidence that the main sources of charge noise in our material platforms are TLFs located

at the native Si/SiO₂ interface. For comparison we also include a relevant data point from recent work performed in Si/SiGe quantum dots by Rojas-Arias *et al.* [28] at 1 mHz (orange star, Fig. 4) where correlations were measured by observing fluctuations in the qubit energy.

Whilst the separation between the qubit and the SiO₂ layer containing TLFs in the Si/SiGe device was comparable at 50 nm, compared to the 45 nm in our Si:P device, there are other substantial differences between our experiment and the work of Ref. [28], including the presence of metal confinement gates and micromagnet in their device. Despite these substantial differences we note that the magnitude of correlations we observe in Fig. 4 from Ref. [28] is in good agreement with our experimental and modeling data pointing to a potential similarity between the noise sources in both systems. Further work is necessary to clarify this point.

III. DISCUSSION

Our results show that in our phosphorus in silicon quantum dot architectures the charge noise observed spatially across multiple dots is highly correlated, in a similar fashion to that observed in superconducting qubit systems. With superconducting qubits, it has been shown that charge noise can be significantly reduced by designing transmon qubits that are only weakly sensitive to charge noise [5]. For semiconductor qubits however, charge noise can couple in a number of different ways. With qubits incorporating a micromagnet, charge noise can couple to the qubit frequency becoming the main source of dephasing noise [15]. Charge noise can also affect the exchange coupling between electron spins, which not only impacts two-qubit gates between electron spin qubits, but also qubits encoded in singlet-triplet states using two-spin encodings [17] as well as exchange-only qubits using three-spin encodings [36]. Recent work [25,27] has also shown that correlations measured in a pair of spin qubits are primarily of electrical origin, providing experimental evidence that the correlations we measure in charge noise will be reflected in the correlations between qubits.

The error-correction threshold exponentially decreases as correlated errors couple to multiple qubits in a 2D array [5], and it is therefore a priority to work in a regime where correlated errors can be effectively eliminated. Based on our measured noise correlations, four parallel routes towards a zero-correlation regime can be pursued: (1) increase the qubit separation distance to reduce the magnitude of correlated noise; (2) increase the frequency at which an error-correction code can be run; (3) optimize the operating conditions to mitigate the effects of qubit errors; and (4) reduce the overall level of charge noise by optimizing materials and device fabrication. In silicon spin qubits, the qubit separation depends on the method of interqubit coupling, usually via

exchange (10's of nm's to 100 nm) or capacitive coupling (100's of nm's). Recent work in long-range qubit coupling [37–39] has been pursued primarily to make qubit architectures modular and more accessible for on-chip integration of control electronics. These advances may simultaneously benefit the suppression of correlated charge noise and its impact on qubit errors. The second route of increasing the frequency at which error-correction codes can be run is achieved through pursuing faster qubit initialization and readout [40] and control [18]. Recent work has shown that noise correlations decrease with increasing frequency [26] in a nonmonotonic manner [28]. While further work is needed to precisely map out noise correlations at higher frequencies than those studied here (> 1 mHz), we anticipate optimal error-correction code operation frequencies exist where noise correlations are minimized. The third proposed solution involves implementing error-mitigation techniques to reduce the impact of correlated errors on quantum computing algorithms. Such methods typically require extracting an accurate noise model of a quantum processor and carefully constructing the circuits such that the errors cancel themselves out [41–43]. Whilst promising, these error-mitigation techniques come with the cost of additional resource and/or time overheads. Finally, the overall impact of correlated noise can be minimized by removing the noise sources from qubit's proximity. Since our results suggest that the correlated noise originates from surface TLFs this can be suppressed in future devices by increasing the thickness of the encapsulation layer between the qubits and these surface oxide TLFs [25,30].

In conclusion, we have measured the power spectral density S and magnitude squared coherence C_{xy} in a linear array of ten quantum dot pairs using simultaneous charge-state peak tracking of four of the quantum dot pairs within the array. We find that correlations in the charge noise are suppressed by increasing the site separation (up to 300 nm), as well as at the higher frequencies (up to 1 mHz) studied in this work. Our experimental findings are supported by analytical modeling, which considers the source of the charge noise as TLFs at the Si/SiO₂ interface. Our modeling replicates the trends observed in our experimental data and recent frequency dependence observed in Si/SiGe quantum dots [26,28]. We observe that the spatial correlations in the Si:P qubit platform decay on the sub- μ m length scale, compared to the approximately mm length scale found in superconducting qubits [5]. These characteristic length scales can be attributed to the different underlying mechanisms causing the correlated noise: for silicon qubits the surface TLFs produce switching charge dipoles on the approximately 10-nm length scale, whereas for superconducting qubits, phonons arising from the absorption of high-energy cosmic radiation leads to a larger spatial footprint of charging events [5,7,9,10]. Phonons in silicon have been shown to affect relaxation and coherence times [44,45], as well as charge-noise levels

[46], however further work is necessary to determine their effect, if any, on charge-noise correlations. Despite the relatively abrupt decay (approximately 300 nm) of spatial correlations observed in our silicon samples, noise correlations pose significant challenges for implementing quantum error-correcting codes. We discuss promising ways to mitigate these either by separating qubits by larger distances, increasing error-correction operation speeds, implementing recent error-mitigation strategies [41–43], and/or improving device fabrication to minimize the known source of noise. In the short term, however, the knowledge gained about the spatially and temporally correlated noise in our semiconductor spin qubits can be leveraged in the NISQ era, where open quantum systems can be computationally powerful [47] and noise correlations have been theoretically shown to improve the performance of variational quantum algorithms [48].

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DATA AVAILABILITY

The data that support the findings of this article are not publicly available upon publication because it is not technically feasible and/or the cost of preparing, depositing, and hosting the data would be prohibitive within the terms of this research project. The data are available from the authors upon reasonable request.

APPENDIX: MATERIALS AND METHODS

1. Device fabrication

Fabrication of the ten quantum dot pair device is performed using scanning tunneling microscopy (STM) hydrogen resist lithography [49–52], where an STM tip is used to selectively desorb a hydrogen mask bound to a 2×1 reconstruction of the (001) silicon surface. This process is performed in an ultrahigh vacuum (UHV) system with a base pressure of approximately 1×10^{-11} mbar. After lithography we dose the surface with phosphine gas (PH₃) at a pressure of 5×10^{-7} mbar for 2 min (1.8 Langmuir) and incorporate the phosphorus atoms into the exposed silicon using a 350 °C anneal for 60 s. The device is encapsulated with a 45-nm-thick layer of epitaxial silicon grown at a temperature of 250 °C and a growth rate of 0.15 nm/min. To electrically contact the device once removed from the UHV environment, silicon vias aligned with STM-defined contact pads are etched using

reactive ion etching and a palladium deposition and subsequent anneal is used to make Ohmic contact with the phosphorus-doped silicon layer.

2. Multiplexed rf setup

All measurements were performed in a dilution refrigerator with a base temperature of 10 mK. The ten quantum dot pair chip was wire bonded to a neighboring multiplexed readout chip based on superconducting thin-film NbTiN spiral resonators. The NbTiN spiral resonators have a nominal track width of 3 μm and pitch of 3 μm . The resonators connected to Q3/Q5/Q6/Q7 have 16/25/32/36 turns, respectively, with outer diameters of 795 μm /903 μm /987 μm /1035 μm . To provide multiplexed rf gate-based charge readout of the bottom dots tunnel coupled to the reservoir leads (R1-R10), each resonator was coupled via an on-chip interdigitated capacitor to a common coplanar strip feedline transmitting a multi-tone rf signal. The resonators were driven with a nominal input power of approximately -95 dBm and the outgoing rf signal was amplified by a 3-K stage low-noise cryogenic preamplifier (CITLF2 Cosmic Microwave technology) with a nominal gain of approximately 30 dB followed by two Pasternak HEMT amplifiers at room temperature with an overall 65-dB gain.

The digital generation, control, and demultiplexed readout of the high-purity multitone signals was implemented using a Keysight PXI M9019A FPGA-based chassis platform with M3201 AWG 500 MS/s DAC and 1 GS/s ADC M3102 digitizer modules. The generated frequency comb with an overall 200-MHz bandwidth was up-converted using a Polyphase AM0350A *IQ* modulator and down-converted after the postamplification chain with a Polyphase AD0105B *IQ* demodulator. The signal was digitally demultiplexed using standard digital lock-in amplification and decimation techniques (a six-state cascaded-integrator-comb filter and a decimation

filter with a down-sampling factor $\times 3000$). The voltage signal-to-noise ratios (SNRs) for the charge transitions (correlated with intrinsic resonators' losses) were approximately equal to 10–20 at 1-kHz postintegration bandwidth being limited down to $\text{SNR} < 2$ above 100-kHz bandwidth by the effective sampling rate of 390 kHz.

The dc voltage bias of the reservoirs (R1-R10) was implemented via RC bias tees, formed by the interdigitated capacitor (3 pF nominal) on the multiplexing chip and the PCB-mounted 1 M Ω metal electrode leadless face (MELF) resistors wire bonded to the DC taps of the spirals.

3. Device characterization

We calculated the charge-noise correlations between sites Q3, Q5, Q6, and Q7. Of the ten quantum dot pairs fabricated these four had the correct combination of frequencies and tunnel rates required for high-quality measurements, as shown in Table I.

Here we summarize the key parameters of the multiplexing chip and the quantum dot pairs connected to them:

(a) Q1: No charge transitions were visible on this quantum dot pair as the resonant frequency f_1 was below the frequency floor of the demodulator (200 MHz).

(b) Q2: While reservoir to dot (RD) charge transitions were seen they were severely attenuated as the resonant frequency was still significantly below the frequency floor of the demodulator.

(c) Q3: RD charge transitions were seen at a resonant frequency $f_3 = 175.1$ MHz by sweeping gates R3 and G3.

(d) Q4: There were no clear charge transitions in the gate space most likely due to the incorrect tunnel rate between the lower quantum dot and the reservoir. The resonant frequency used is $f_3 = 213.9$ MHz.

(e) Q5: RD charge transitions were seen at a resonant frequency $f_5 = 251.7$ MHz.

TABLE I. Summary of the key parameters of the multiplexing chip. The resonant frequency f_0 and quality factors—total (internal, external)—are calculated using S21 data. Gate leakage ranges are presented as between the reservoir|gate, and were measured out to 2 V. Visible charge transitions are labeled as either reservoir to dot (RD) or interdot (ID).

Qubit	f_0 (MHz)	Q_t (Q_i , Q_e)	Leakage R G	Transitions
1	—	—	$-0.7:0.9 \mid -2.0:2.0$	—
2	129.8	130 (133, 1885)	$-0.8:1.1 \mid -0.5:0.8$	—
3	175.1	190 (227, 1096)	$-0.5:1.2 \mid -1.0:1.2$	RD
4	213.9	273 (461, 661)	$-0.7:1.1 \mid -2.0:2.0$	—
5	251.7	293 (660, 421)	$-0.8:1.0 \mid -0.9:1.1$	RD, ID
6	317.6	593 (1863, 789)	$-0.6:0.9 \mid -0.6:1.0$	RD, ID
7	374.3	335 (1968, 330)	$-0.6:0.7 \mid -0.6:1.0$	RD
8	414.2	362 (1753, 398)	$-0.7:1.1 \mid -2.0:2.0$	RD
9	493.5	4246 (5071, 20416)	$-0.7:1.1 \mid -1.1:1.9$	—
10	552.7	251 (1486, 302)	$-0.9:1.2 \mid -2.0:2.0$	—

(f) Q6: RD charge transitions were seen at a resonant frequency $f_6 = 317.6$ MHz.

(g) Q7: RD charge transitions were seen at a resonant frequency $f_7 = 374.3$ MHz.

(h) Q8: While three RD transitions were visible at a resonant frequency $f_8 = 414.2$ MHz, a small tip drop occurred during STM lithography between the quantum dots making the results incomparable.

(i) Q9: Whilst the bond wire to the multiplexing chip remained connected as evidenced by the order of magnitude higher quality factor compared to chip-bonded resonators, the bond wire to the device became disconnected during cool down.

(j) Q10: Gate G10 was disconnected during cool down.

To avoid the device going into leakage (where current flows between control gates), we only scanned voltage ranges between -0.3 and 0.1 V, remaining well within the leakage range of each gate (-0.8 to $+1.1$ V). When the device does go into leakage it must be warmed from mK to above the charge freeze-out temperature of the carriers which for silicon is approximately 60 K. Warm up is a slow procedure so the risk of entering leakage was mitigated for all these measurements.

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