

Nanoscale wireframe SQUID on a cantilever by corner lithography

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We present the fabrication of nanoscale superconducting quantum interference devices (SQUIDs) at the apex of wireframe tips on self-aligned superconducting cantilever probes. The probes are made on silicon wafers using molding techniques in combination with corner lithography, which results in a nanowire frame tip with a tunable apex structure. A shadow-effect deposition using magnetron sputtering of niobium creates self-aligned superconducting wireframes on cantilevers with accompanying device circuitry. Superconducting weak links are realized at the apex of the wireframes with the use of focused ion beam nanopatterning. The realized SQUIDs have effective diameters ranging from several micrometers down to 100 nm and can be operated in magnetic fields up to 1 T. Furthermore, the nanowires in the wireframe can be used to flux modulate the SQUID locally. This fabrication process enables the production of wafer-scale templates for probes based on on-tip superconducting devices.

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Superconducting quantum interference devices (SQUIDs) are the sensors with the highest magnetic-field sensitivity [1–5]. In scanning SQUID microscopy (SSM), SQUIDs are used for nanoscale magnetic imaging. Here, one uses a SQUID to locally map and image the magnetism in a sample [6–9]. Among others, SSM has been used to image the order-parameter symmetry in high- T_c superconductors [10–13], the interplay between magnetism and superconductivity at oxide interfaces [14,15], currents in topological insulators [16–18], ferromagnetic domain patterns in magnetic oxides [19–21], Abrikosov vortices in type-II superconductors [22–25], and local dissipation in the quantum Hall state in graphene [26,27].

In the past decades, much effort has been dedicated to the development of SQUID probes for SSM, with the main focus to increase spatial resolution while maintaining high magnetic-field sensitivity [8,9,28]. Traditionally, SQUID probes for SSM have been realized in large quantities on planar silicon wafers by conventional lithography [29–31]. These SQUID-on-chip probes have the advantage of additional on-chip circuitry such as flux modulation coils, a pickup loop, and coils to measure magnetic susceptibility, which together extend the functionalities of these

SQUIDs. However, scanning in close proximity to the sample is hindered by the planar structure of the substrate chip, and the spatial resolution is typically limited to only several micrometers [8,9].

To improve the spatial resolution of a SQUID probe, one has to bring the SQUID in closer proximity to the sample surface and reduce its effective area. This can be done by raising the SQUID onto an elevated surface like a sharp tip; the SQUID-on-tip probe was the first SQUID probe to achieve this [32,33]. Here, a three-step thermal evaporation of a superconductor onto a pulled quartz capillary creates a self-aligned SQUID at the apex of a sharp tip. This method allows for the fabrication of the smallest SQUID sensors to date [34] and, by using conventional scanning probe feedback, for scanning within close proximity to the surface, increasing the spatial resolution to below 100 nm [35,36]. However, the current SQUID-on-tip fabrication process hinders scalability; in addition, the geometry of the quartz capillary precludes the addition of auxiliary circuitry.

On the other hand, focused ion beam (FIB) milling on planar substrates has been an established technique to create nanoSQUIDs [37–42] and can be used in combination with atomic force microscopy (AFM) cantilever probes to create SQUID probes [43–45]. This fabrication method is highly versatile as it takes advantage of the precise nanoscale modification offered by FIB alongside the superior topographical feedback provided by AFM.

Here, we combine wafer-scale molding and preparation of self-aligned superconducting cantilever probes with the

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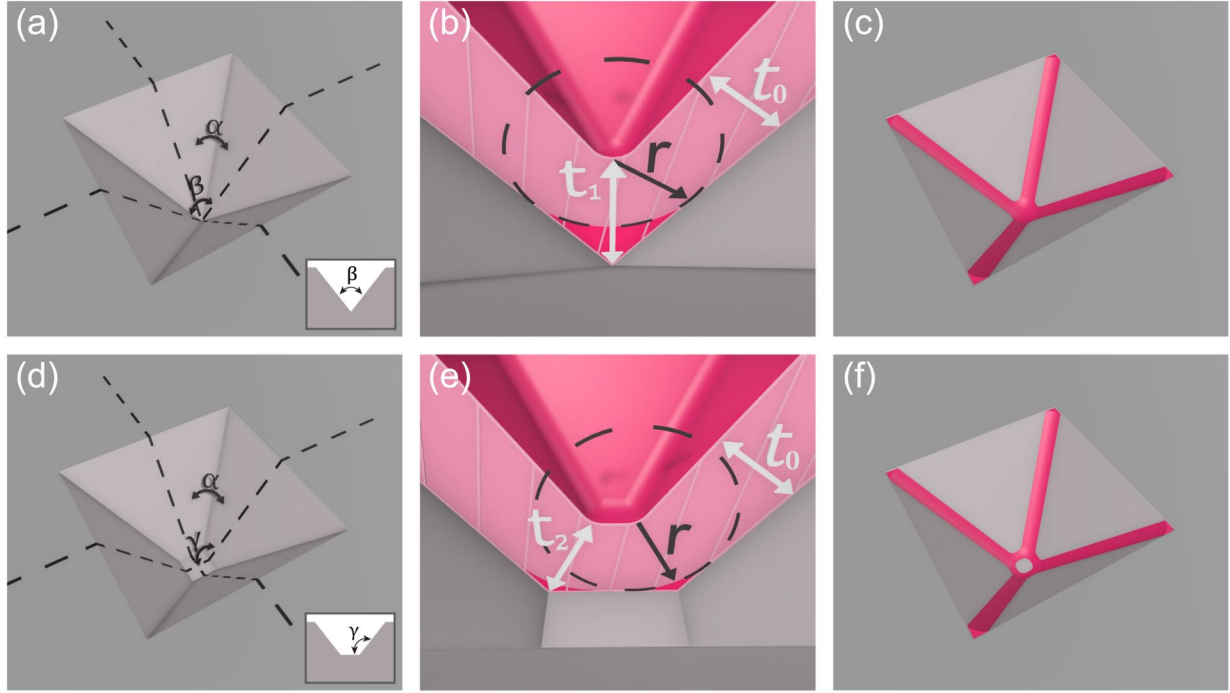


FIG. 1. Schematic of the principle of corner lithography. (a) and (d) Template preparation consisting of pits with concave corners α , β , and γ . The inset shows the angle between the planes at the bottom of the pit. (b) and (e) Enlarged image of the conformal layer deposition (cross section) at the pit bottom of (a) and (d). The thickness in the corners (t_1 and t_2) exceeds the conformal layer thickness (t_0). After corner lithography, with an isotropic thinning distance r , nanostructures are formed in the corners of the template. (c) and (f) Corner lithography is able to make complicated three-dimensional structures by combining the nanostructures formed in different corners of the template with each other. The top (a)–(c) and bottom (d)–(f) rows highlight that a variation in the initial template results in different nanostructures after the corner-lithography process.

patterning of weak links using a FIB to create nanoscale wireframe SQUID on cantilever probes. Nanowire frame tips with either open loops or sharp apices attached to predefined electrodes on a cantilever are made using corner lithography and standard microfabrication processes. Self-aligned superconducting probes are created by a shadow-effect deposition of Nb by magnetron sputtering. A single step of FIB milling is used to create superconducting weak links at the apex of the tip, forming a SQUID-on-tip. The loop size of the SQUIDs can be controllably varied, from several micrometers down to 100 nm. The SQUIDs can be operated in magnetic fields up to and exceeding 1 T, and on-tip flux modulation can be supplied using the nanowire electrodes. Our approach shows the possibility of preparing and creating versatile scanning probes based on superconducting devices on the wafer scale.

Corner lithography is a versatile nanofabrication technique and has been used for wafer-scale fabrication of complex three-dimensional structures [46–57]. The technique of corner lithography is schematically illustrated in Fig. 1. It consists of three basic steps: First, a template is created that contains concave corners, such as the inverted pyramid in Figs. 1(a) and 1(d), with corners of angles α , β , and γ . Second, a conformal deposition of material is performed that follows the geometry of the underlying

template. The deposited layer will be thicker than the conformal layer thickness (t_0) in the corners of the template, as can be seen in Figs. 1(b) and 1(e). Finally, the conformal layer is selectively etched for an isotropic thinning distance r using time-controlled isotropic etching. This forms nanostructures in the corners with a thickness given by $t_0 / \sin(\theta/2) - r$, where θ is the angle of the corner [Figs. 1(b) and 1(e)].

Corner lithography results in the formation of a nanowire for the angles α and γ (formed by the intersection of two planes), whereas for the angle β (created by the intersection of four planes at the apex of the inverted pyramid), a nanodot will be formed. By combining these different angles with one another, one can connect different nanofeatures together to create a self-aligned three-dimensional structure [49]. In Fig. 1(a), the sharp inverted pyramid template results after corner lithography in a frame of nanowires that coalesces in a sharp dot, as shown in Fig. 1(c). However, by only slightly adjusting the template to an inverted truncated pyramid [Fig. 1(d)], the tip structure changes to a frame of nanowires connected to a square loop of nanowires; see Fig. 1(f). This shows the versatility that is offered by corner lithography to make complicated three-dimensional nanostructures by variations in the initial template.

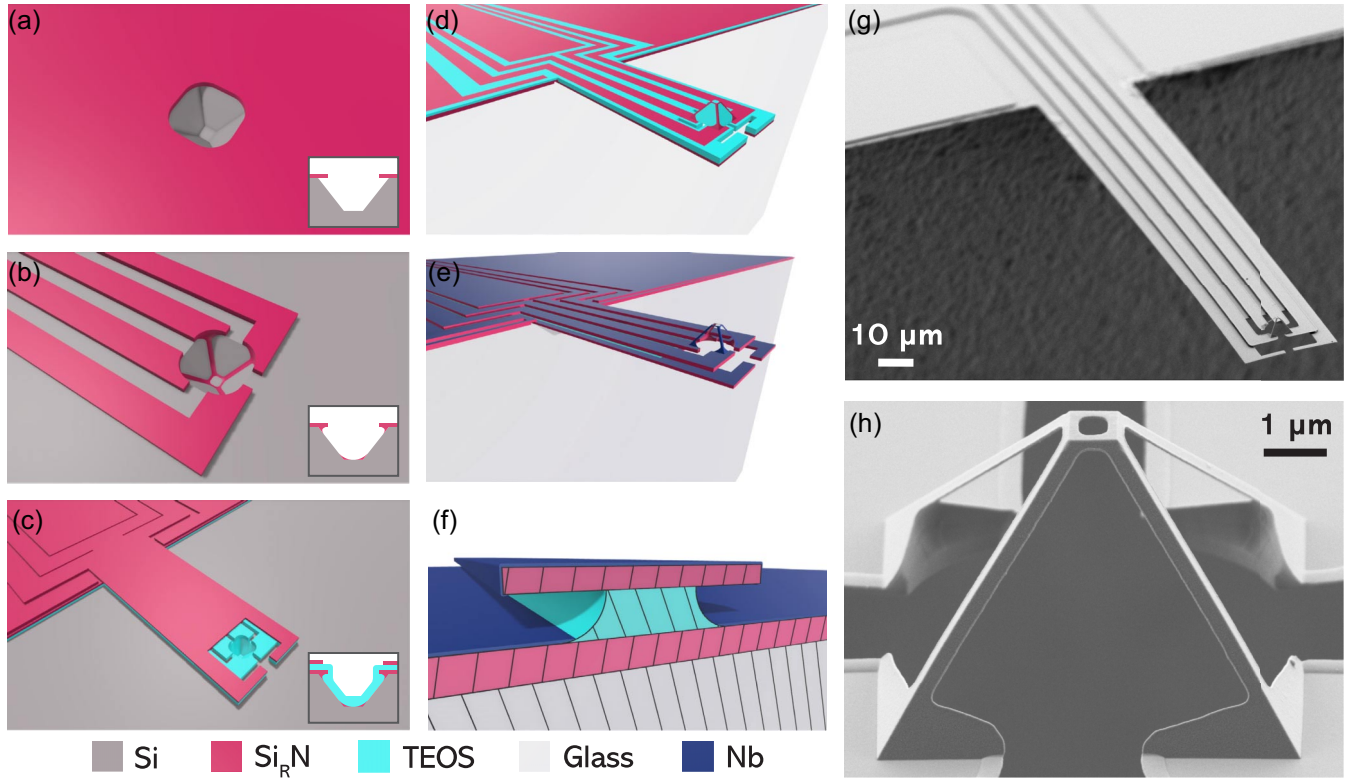


FIG. 2. (a) Etched inverted truncated pyramid in Si (100), defined by a rounded silicon-rich nitride (Si_RN) mask. (b) Etching of electrodes in the Si_RN mask, subsequent corner lithography is performed with an additional conformal layer of Si_RN to create a wireframe with an open loop, which is connected to the electrodes. (c) Deposition of a heterostructure of TEOS/ Si_RN /TEOS (second tetraethyl orthosilicate (TEOS) layer not shown) and subsequent lithography and etching to define the cantilever and chip layout. The insets in (a), (b), and (c) show a cross-sectional view of the silicon pit. (d) Anodic bonding of a diced glass wafer to the top TEOS layer, subsequent etching of the Si wafer in tetramethylammonium hydroxide (TMAH) to release the freestanding cantilever probe [chip is flipped upside down with respect to (c)]. (e) Magnetron sputtering of Ti/Nb/Pd/Au on the entire chip creates a self-aligned superconducting probe. (f) Cross-section image of the TEOS undercut and shadow-effect deposition to electrically separate the Si_RN chip and electrode layers. (g) Scanning electron microscopy (SEM) image of the created self-aligned superconducting cantilever probe with a tip at its end. (h) SEM image of the open-loop superconducting wireframe tip.

The process to fabricate the self-aligned superconducting wireframe on cantilever probes is shown in Fig. 2. First, templates for corner lithography are created in silicon (100) wafers. We deposit a 400-nm-thick low-stress Si_RN layer on a Si (100) wafer using low-pressure chemical vapor deposition (LPCVD). Square openings are defined in the Si_RN by optical lithography and reactive-ion etching (RIE). To define templates for corner lithography, we use anisotropic etching of silicon in potassium hydroxide (KOH), which results in the formation of inverted pyramids defined on the sides by the crystal (111) planes of the silicon. By controlling the etching time, one can either make sharp inverted pyramids, where the four (111) planes intersect into a sharp apex [Fig. 1(a)], or by prematurely stopping the etching, one can create an inverted pyramid bound by a square bottom (100) plane [Figs. 1(d) and 2(a)]. Here, the dimensions of the initial mask opening and etching time define the size of the square bottom, which can be varied from tens of nanometers to several

micrometers. Next, optical lithography is used to define electrodes and contact pads in the Si_RN mask, which connect to the four corners of the inverted pyramid. Subsequently, a conformal layer of Si_RN is deposited using LPCVD. Corner lithography is performed on this 500-nm-thick Si_RN layer by time-controlled selective isotropic etching in hot H_3PO_4 . We overetch the Si_RN layer by 5% (overetch factor = 1.05), which ensures that corner lithography forms nanowires in the ribs of the inverted pyramid [52] and nanowires in the ribs of the square bottom. If desired, a nanodot at the apex of the sharp inverted pyramid can also be formed. Since the Si_RN electrode layer overlaps with the inverted pyramid, the nanowire frame is physically connected to the electrodes; see Fig. 2(b) for the result. Next, we deposit a trilayer of TEOS (700 nm), Si_RN (400 nm), and TEOS (110 nm) using LPCVD and the cantilever structure and chip layout are defined by optical lithography and RIE; see Fig. 2(c). Using anodic bonding a glass wafer with prediced trenches

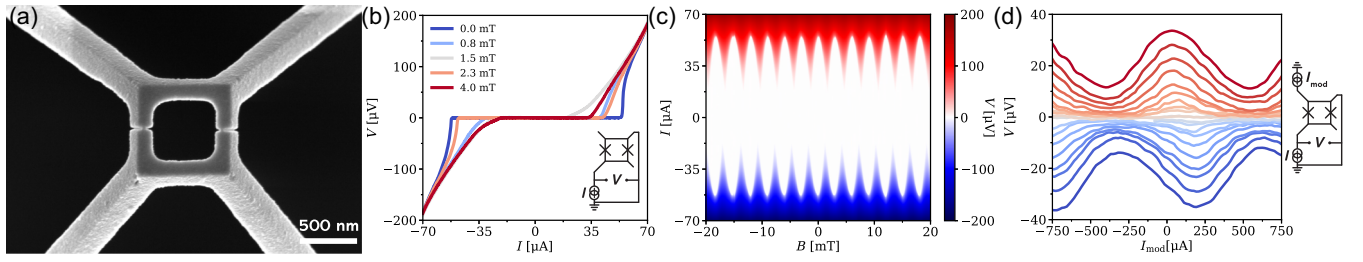


FIG. 3. (a) Scanning electron microscopy image of a SQUID at the apex of an open-loop nanowire frame tip; the two Dayem bridges milled with FIB are also visible. (b) Current-voltage characteristics at 6.5 K for different applied fields; on the right, a schematic is shown of the measurement circuit. (c) Quantum interference pattern of the SQUID. (d) On-tip flux modulation by a modulation current supplied with one of the nanowires in the wireframe; see the schematic on the right. The SQUID voltage oscillations can be seen for the applied modulation current for various bias currents (-100 to 100 μA with steps of 10 μA) at $T = 6$ K.

is bonded to the silicon wafer, where we ensure the cantilevers are not covered by the glass wafer and instead extend over the trenches. In order to release the cantilever and corner-lithography-defined nanowire frame tip, the remaining glass above the cantilever is removed by dicing, and consequently, the entire silicon wafer is selectively etched using TMAH; see Fig. 2(d) for the resulting freestanding cantilever probe.

The thick TEOS layer, which is sandwiched between the bottom Si_3N_4 cantilever and chip layer and top Si_3N_4 electrode layer, is selectively etched using buffered hydrofluoric acid to create a physical undercut between the cantilever and electrode Si_3N_4 layers. This undercut creates a shadow effect between the two Si_3N_4 layers. The shadow effect will transfer to any superconducting layer deposited on the entire probe, ensuring electrical separation of the device circuitry from the rest of the chip; see Fig. 2(e) for the superconducting cantilever probe and Fig. 2(f) for an enlarged cross-section image of the shadow-effect deposition. Because the large physical undercut, it is also possible to use a less directional deposition technique, such as sputtering, to create a self-aligned superconducting probe. Conventional magnetron sputtering is then used to deposit a 5 nm adhesion layer of Ti, a 60 nm layer of superconducting Nb, a 2 nm capping layer of Pd, and finally a 20-nm-thick layer of Au (gold) to serve as a protection layer during FIB. The final self-aligned superconducting cantilever probe, shown in Fig. 2(g), has contact pads and electrodes on the glass chip base, and electrodes connect to the wireframe tip that extend onto a 150 μm -long by 30 μm -wide cantilever; see Fig. 2(h). Using this technique wireframe tips with open-loop sizes of several micrometers down to 300 nm have been made on the wafer scale; see Appendix A. Moreover, by using multiple steps of corner lithography [50,51] or by using a thinner initial thickness of the conformal layer, the size of the created open loops can be reduced further.

We have characterized the mechanics of the superconducting cantilever probes at room temperature and in air; see Appendix B. The cantilever probes have low dynamic spring constants of 0.2 – 0.3 N/m. This would

make them suitable for contact- or intermittent-contact mode AFM since they exert little force, minimizing damage to the tip and sample. In order to show that the fabricated superconducting probes are sufficiently rigid and can also be used for scanning probe microscopy, we have tested the probes in a room-temperature commercial AFM system. See Fig. 7 in Appendix C for an AFM image taken in intermittent-contact mode of highly oriented pyrolytic graphite (HOPG). The probe is able to resolve the step edges of the HOPG and does not deteriorate during tapping-mode scanning, thus showing its robust use for scanning probe microscopy.

In order to create a SQUID at the nanowire frame tip, FIB milling with Ga ions is used. This allows for the direct patterning of electrical circuitry at the tip of the probe. Figure 3(a) shows constriction junctions in the nanowires of the open-loop wireframe milled by FIB. The FIB milling required to make the bridges is minimal, allowing the use of low beam power and short milling times. This reduces the amount of Ga that is implanted into the superconducting Nb, thus preserving the high critical temperature of Nb [37]. Figure 3(b) shows the current-voltage characteristics of one of the FIB-milled SQUIDs. The I - V characteristics are measured using a simple current-bias scheme at a temperature of 6.5 K for different perpendicular magnetic fields. The I - V characteristics of the SQUID show no hysteresis at this operating temperature. However, when the temperature is decreased, the device will exhibit a hysteretic dependence, which we attribute to Joule heating in the constriction junctions by high critical currents [58,59]. The I - V characteristics show a significant modulation of the critical current for an externally applied field, $I_c(B)$, of tens of μA . Figure 3(c) shows the quantum interference pattern associated with the I - V characteristics from Fig. 3(b). The oscillation period of the pattern is 2.98 mT, which corresponds to an effective SQUID area of 0.69 μm^2 and an effective square-loop SQUID size of 833 nm. Figure 8 in Appendix D shows three additional open-loop nanoSQUIDs with different effective areas. The smallest open-loop nanoSQUIDs that we have made have dimensions of 472 nm and a SQUID

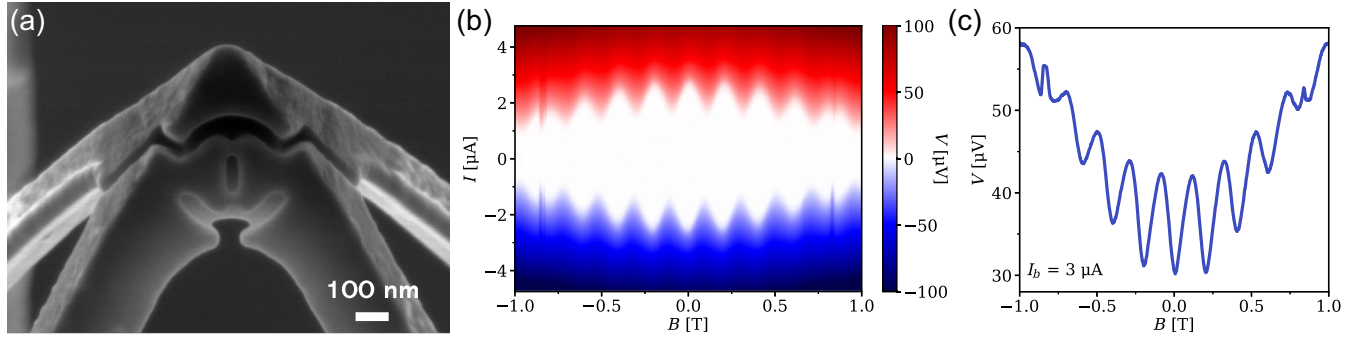


FIG. 4. (a) Scanning electron microscopy image of a completely FIB-made nanoSQUID on a sharp nanowire frame tip. (b) Quantum interference pattern of a nanoSQUID with an effective diameter equal to 114 nm taken at a temperature of 3.25 K. The applied magnetic field is perpendicular to the cantilever probe. (c) SQUID oscillations in the normal state at $I_b = 3 \mu\text{A}$ for a large range of magnetic field.

area of $0.22 \mu\text{m}^2$; this exceeds the geometrical hole area of the smallest open-loop wireframe (Fig. 8 in Appendix D). We attribute this difference to flux focusing of the nanowires in the open-loop wireframe, which increases the effective area of the SQUID.

From the modulation of the critical current $I_c(B)$, one can calculate the SQUID inductance parameter β_L using $1/(1 + \beta_L) = \Delta I_c/I_{c,\text{max}}$, assuming that the current-phase relationship is sinusoidal [60]. We find $\beta_L = 0.53$, and from $\beta_L = 2LI_c/\Phi_0$, we estimate the SQUID inductance to be 20 pH, of which the main contribution originates from the kinetic inductance of the constriction junction bridges [4,61,62]. To characterize the sensitivity of the SQUID probes, we measure the flux noise spectral density of the SQUID at several applied magnetic fields; see Fig. 9 in Appendix E. For a large range of frequencies, the lowest measured white flux noise floor was $3.8 \mu\Phi_0/\sqrt{\text{Hz}}$. This is consistent with SQUID systems lacking feedback loops or cryogenic amplification, where the noise profile is primarily limited by the room-temperature voltage amplification [2,4,5,63].

As indicated by the schematic in Fig. 3(b), only two of the four nanowires in the wireframe are used for the current-bias readout. Hence, the remaining nanowires can be used to extend the functionalities of the on-tip circuitry. By using a shared ground, a modulation current I_{mod} can be supplied using a nanowire electrode in addition to the bias current. As can be seen from the SQUID voltage oscillations in Fig. 3(d), the extra modulation current can be used to effectively flux-bias and modulate the wireframe SQUID. We can calculate the mutual inductance between the nanoSQUID and modulation line using $M = \Phi_0/\Delta I_{\text{mod}}$. For the measured oscillation period of $\Delta I_{\text{mod}} = 925 \mu\text{A}$, we find $M = 2.23 \text{ pH}$. However, note that due to the strong modulation current used, this also produces a significant stray field in close proximity to the tip.

The use of on-tip flux modulation allows for integrating the wireframe SQUID on a cantilever together with a

flux-locked loop to increase its sensitivity and operating range [2,7]. Additionally, the flexibility of FIB to mill an extra constriction bridge allows for operating the SQUID in a superconducting phase-locked loop [44,64]. In essence, the existence of the extra two nanowire electrodes allows for further extending the functionalities of the probe with additional on-tip circuitry [8].

As discussed earlier in Fig. 1, slightly altering the initial template mold formed by KOH etching at the start of the fabrication changes the final tip structure. Changing from a KOH etch with a flat square bottom to one with a sharp point, as illustrated in Fig. 1(a), the final tip structure is also changed to a nanowire frame that coalesces into a sharp dot; see Fig. 1(f). The FIB can be used in a similar fashion as in Fig. 3(a), but this time to pattern the entire SQUID circuitry, including the nanoconstrictions, SQUID hole, trenches to reduce flux focusing, and leads to connect the SQUID to the electrodes from the wireframe. In that case, the SQUID dimensions that can be realized are not limited to the wafer-scale fabrication process but to the resolution of the FIB. Hence, smaller nanoSQUIDs can be made like the one shown in Fig. 4(a). Figure 4(b) shows the nanoSQUID quantum interference pattern with an oscillation period of 203 mT, which corresponds to an effective SQUID area of $0.01 \mu\text{m}^2$ and a diameter of 114 nm. The pronounced $I_c(B)$ oscillations survive up to high fields, even above 1 T. In addition, the voltage oscillation at a given bias current, Fig. 4(c), also exists over a wide range of magnetic fields. Also note the small jumps both in the $I_c(B)$ in Fig. 4(b) and the voltage oscillations in Fig. 4(c) at $\pm 0.8 \text{ T}$. We attribute these jumps to the entry of a vortex in the wireframe loop and coupling into the nanoSQUID [65]. The SQUID patterned on the side of a sharp wireframe tip also has influence on the scanning capabilities of the probe. Since the sensitive SQUID is not at the apex of the tip, it will be protected during contact or intermittent-contact scanning AFM modes. However, a downside is reduced spatial resolution

since the SQUID will always be at a distance of half the diameter of the SQUID loop away from the point of contact, which effectively increases the scanning height of the SQUID [28]. In addition, because the sharp nanowire frame tip is molded in the silicon crystal, the angles of the nanowires with respect to the cantilever plane are well defined at 54.3° . Hence, in comparison to the in-plane SQUID shown in Fig. 3(a), a FIB-milled SQUID at the side of the tip, as shown in Fig. 4(a), is sensitive to both the in- and out-of-plane components of the magnetic field. Thus, the wireframe nanoSQUID probe can be easily altered to fit the specific experiment to be performed or magnetic source to be measured. For instance, for currents, which produce both in- and out-of-plane magnetic fields, the sharp wireframe SQUID may be a better probe due to its sensitivity to both magnetic-field directions [15,45].

In summary, SQUIDs at the apex of wireframe tips defined by corner lithography have been created using focused ion beam milling. These SQUIDs on tips are integrated into self-aligned cantilever probes with on-chip device circuitry realized with shadow-effect deposition on the wafer scale. The tip structure created by corner lithography can be easily modified by varying the initial mold. The versatility offered by both FIB and corner lithography allows for the fabrication of a wide range of SQUIDs with diameters ranging from several micrometers down to 100 nm, which can be operated in large external magnetic fields. Furthermore, since the wireframe tip is composed of four individual nanowires, one can use two of the nanowire electrodes to provide on-tip modulation of the SQUID. The bottom-up wafer-scale fabrication process to create the wireframe SQUID on a cantilever probe enables integration of future piezoresistive on-chip sensing of the cantilever feedback during scanning [66]. This will make the SQUID on cantilever a suitable probe for scanning probe microscopy in cryogenic environments, where optical AFM feedback is challenging.

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The Bruker Nano Surfaces and Metrology Division develops and sells probes and associated measurement equipment similar to what is described in this paper.

DATA AVAILABILITY

The data that support the findings of this article are openly available [67].

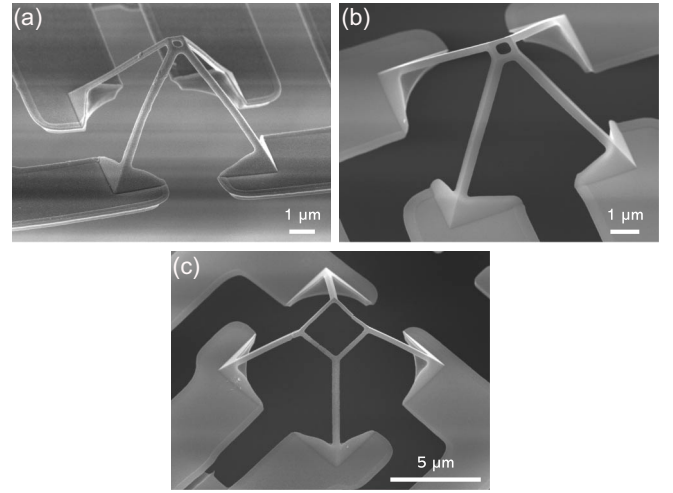


FIG. 5. SEM images of open-loop wireframe tips on cantilevers with various hole dimensions of the open loop: (a) 320 nm, (b) 460 nm, and (c) 2.3 μm .

APPENDIX A: SUPERCONDUCTING OPEN-LOOP WIREFRAME TIPS

The wafer-scale fabrication process to create the superconducting cantilever probes described in the text can create open-loop wireframe tips over a large range of dimensions from several hundred of nanometers to a few micrometers. In Fig. 5, we show three additional open-loop wireframe tips across this range. The smallest realized open-loop wireframes have a hole size of approximately 300 nm, whereas the largest can be multiple micrometers in size. In addition, the yield of the wafer-scale fabrication process is high. We estimate from SEM imaging that approximately 80%–90% of all devices have intact wireframe tips. We believe that by optimization of the fabrication process, this number can be increased further.

APPENDIX B: CANTILEVER MECHANICS

We have characterized the mechanics of the cantilever probes using a laser vibrometer (MSA-600 Micro-System

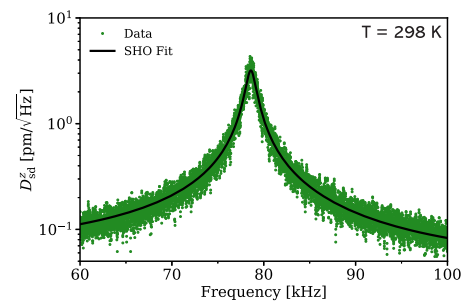


FIG. 6. Displacement spectral density measured for the fundamental mode of a superconducting cantilever probe in air. The data are fit using a simple-harmonic oscillator (SHO) model from Ref. [68].

Analyzer from Polytec). We measured the cantilever displacement noise around the fundamental resonance mode at room temperature and in air; see Fig. 6. Thermal noise will result in small fluctuations of the cantilever, which can be approximated by using a simple-harmonic oscillator model [68,69]. From this model, one can extract several properties of the cantilever such as its resonant frequency (fundamental mode), Q-factor, and spring constant. For our probes, we find resonant frequencies in the range of 70–100 kHz, Q-factors (in air) between 60 and 90, and a spring constant of 0.2–0.3 N/m. In addition, the bottom-up fabrication allows for control of the cantilever properties to match the desired AFM scanning mode.

APPENDIX C: ROOM-TEMPERATURE ATOMIC FORCE MICROSCOPY

The AFM measurements shown in Fig. 7 were done using a commercial Dimension Icon AFM from Bruker. A sharp wireframe tip cantilever probe was used for the AFM measurements shown. In order to use optical feedback during AFM scanning, a reflective coating of 5 nm Ti and 30 nm Au was sputtered on the backside of the cantilever. The topography of HOPG was imaged using peak-force tapping-mode AFM, a dynamic technique where an oscillating cantilever allows the tip to intermittently contact the sample surface. The smallest observed step edge in Fig. 7(b) has a height of 0.7 nm, which equals two graphite monolayers [70,71]. Most significantly, during and after AFM, the probes showed no signs of deterioration, demonstrating the robustness of the design.

APPENDIX D: ADDITIONAL QUANTUM INTERFERENCE PATTERNS OF WIREFRAME SQUID ON CANTILEVER PROBE

Beyond achieving high yields in wafer-scale fabrication, we have also optimized our FIB process to ensure a high SQUID fabrication yield. Our current process ensures that nearly all FIB-fabricated SQUID devices are functional. To illustrate this, we show additional quantum interference patterns of three different wireframe SQUIDs in Fig. 8

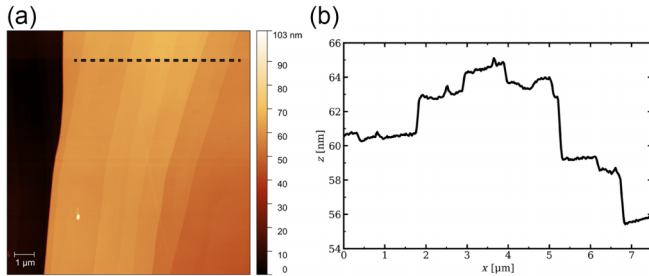


FIG. 7. (a) Peak-force tapping-mode AFM image taken of the topography of HOPG. (b) Linescan associated with the dashed line in (a), which shows the step edges of the HOPG terraces.

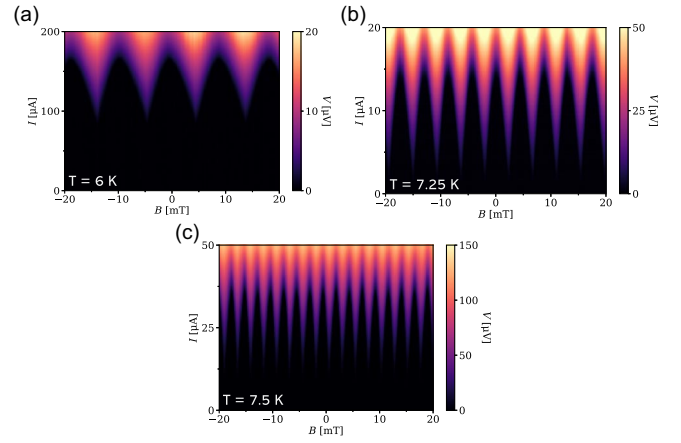


FIG. 8. Quantum interference patterns for nanoSQUIDs on open-loop wireframe tips with different sizes and oscillation periods. (a) $\Delta B = 9.3$ mT and $d = 472$ nm, (b) $\Delta B = 4.3$ mT and $d = 693$ nm, and (c) $\Delta B = 2.4$ mT and $d = 928$ nm.

with different loop sizes. Since both the hole and the flux focusing of the superconducting nanowires in the open loop contribute to the effective SQUID area, we approximate the SQUID to be rectangular. Therefore, we use $d = \sqrt{\Phi_0/\Delta B}$ to calculate the SQUID sizes in Fig. 8.

APPENDIX E: FLUX NOISE OF WIREFRAME SQUID ON CANTILEVER PROBES

To characterize the sensitivity of the wireframe SQUIDs, the flux noise spectral density was measured and is shown in Fig. 9. At low frequencies, below 3 Hz, there is a clear $1/f$ noise contribution. A large amount of microphonic pickup below 1 kHz was observed in Fig. 9(a). This was significantly reduced in Fig. 9(b) by twisting the measurement wires. Further, for a large frequency range from 10 Hz to 40 kHz, a white noise floor is observed with a level between 100 and $3.8 \mu\Phi_0/\sqrt{\text{Hz}}$, depending on the background field. With our SQUID area of $0.69 \mu\text{m}^2$, this corresponds to a field

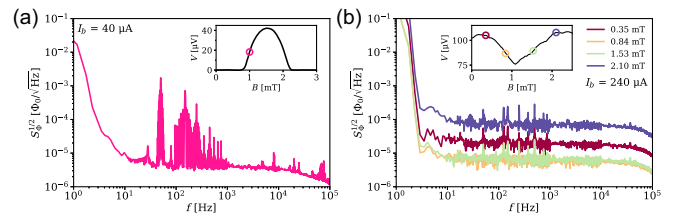


FIG. 9. Flux noise spectral density measured for the open-loop wireframe SQUID (main article Fig. 3). (a) Flux noise spectral density at $I_b = 40 \mu\text{A}$, 6.5 K, and 1 mT. The inset shows the voltage response of the SQUID. (b) Flux noise spectral density at different applied fields taken at 4.5 K. The inset shows the voltage response at $I_b = 240 \mu\text{A}$; the colored circles indicate the points at which the spectra were taken.

noise of 300 to 11.4 nT/ $\sqrt{\text{Hz}}$ over a large range of applied fields.

Our flux noise is comparable to most SQUID setups that make no use of low-temperature amplification or feedback loops [2,4,5]. Our measured minimum flux noise is still 2 orders of magnitude larger than the quantum noise limit, which for our SQUID with an inductance of 20 pH is given as $S_{\Phi_0, \text{QNL}}^{1/2} = \sqrt{\hbar L} = 22 \text{ n}\Phi_0/\sqrt{\text{Hz}}$ [7,60]. However, we attribute this difference to the dominant noise from the room-temperature voltage amplification [63]. The amplifier has a white noise floor of approximately 1 nV/ $\sqrt{\text{Hz}}$, which is equivalent to $3.57 \mu\Phi_0/\sqrt{\text{Hz}}$ using our highest SQUID transfer function of $280 \mu\text{V}/\Phi_0$ [inset of Fig. 9(a)].

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