

High-power test of normal conducting cavities with real-time resonant frequency tracking

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Normal-conducting radio frequency cavities are essential in particle accelerators, but their operational stability is often compromised by thermal-induced resonant frequency detuning during high-power operation. This paper introduces a digital low-level radio frequency system that performs autonomous frequency tracking and compensation in a standalone configuration. Specifically, during powering up and rf conditioning, the tracking operates without dependence on external instrumentation. The system employs a vector modulator driven by two orthogonal analog sinusoids of equal amplitude to modulate the reference signal, achieving an adjustable output bandwidth of ± 1.56 MHz with a precision of 95.3 Hz entirely within the LLRF framework. A phase-locked loop controller embedded in the system dynamically synchronizes the rf frequency to the cavity resonance, while a real-time spectrum analyzer implemented in the FPGA monitors frequency deviations in a closed-loop manner. Experimental results verify that the system can resolve spectral components within a 1.56-MHz bandwidth and generate arbitrary-frequency rf signals over a 3-MHz span using only its integrated LLRF resources. In high-power tests, the embedded PLL-based tracking maintained the reflected power at 8.5% of the incident power under thermal detuning exceeding 200 kHz, thereby ensuring operational stability through a unified LLRF-based approach.

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I. INTRODUCTION

Normal-conducting radio frequency (rf)¹ cavities [1] remain a cost-effective and low-maintenance solution for particle accelerators. By elongating electron bunches in storage rings, they help extend beam lifetime [2]—a key reason for their continued use in major synchrotron facilities such as the Shanghai Synchrotron Radiation Facility (SSRF) [3] and the European Synchrotron Radiation Facility (ESRF) [4]. Building on years of expertise in this field, our team has designed and manufactured a single-cell normal-conducting cavity. Its key parameters are summarized in Table I, with the picture provided in Fig. 1 [5]. Furthermore, rf conditioning and high-power testing are essential prior to its installation in the facility.

To ensure reliability during rf conditioning and long-term operation, this cavity relies on a digital low-level radio frequency (LLRF) control system. This system executes four critical functions: precise control of rf power (amplitude, phase, and frequency), real-time waveform display and parameter configuration, instantaneous breakdown protection, and fully automated rf power ramping. By maintaining stability under dynamic conditions and responding to faults within microseconds, the LLRF system ensures both operational efficiency and hardware longevity.

As rf power input to the normal-conducting cavity ramps from 0 to 50 kW in continuous wave (cw) over several minutes, ohmic losses in the copper cavity walls induce thermal expansion. This expansion increases the physical dimensions of the cavity, resulting in a downward shift in resonant frequency [6]. As per the cavity's design parameters, a temperature rise of 30°C during operation correlates with a resonant frequency detuning of approximately 200 kHz. During rf conditioning, dynamic adjustments to the input power exacerbate this frequency instability, causing rapid fluctuations that far exceed the cavity's 15-kHz operational bandwidth. Such a mismatch—spanning hundreds of kilohertz—would critically degrade system performance. To maintain stable operation, an active compensation mechanism is required: either the rf generator frequency or the

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¹All the abbreviations used in this paper are summarized in Table II.

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TABLE I. rf design performance of the cavity.

Parameters	Values
Frequency	499.654 MHz
Voltage	600 kV
Quality factor	31 880
Shunt impedance	3.7 M Ω
Power loss	50 kW
Accelerating gradient	1.6 MV/m
Operating mode	TM01 continuous wave

cavity's resonant frequency must be continuously tracked and adjusted to ensure synchronization.

Two primary methods exist for frequency tracking in rf systems: adjusting the rf generator frequency (via a reference signal) and mechanically tuning the cavity (using a tuner). While theoretically viable, both approaches face critical limitations in practice—particularly during rf conditioning or in operating facilities—due to inherent technical and operational constraints.

For rf reference source adjustments: (1) Labor intensity: Locating the cavity's resonant frequency necessitates expert intervention. During rf conditioning, operators must manually monitor reflected power and perform iterative adjustments to the signal generator—a Sisyphean task that demands constant attention. (2) Operational impracticality: Within large accelerator complexes, the reference sources act as a universal reference for all subsystems and are predetermined at the facility's design stage. Therefore, their operating frequency is fixed and cannot be modified exclusively for the benefit of the rf system.

For mechanical cavity tuning: (1) Reliability risks: Frequent repositioning of the tuner accelerates mechanical wear, increasing the likelihood of failures in critical components. (2) Speed limitations: Mechanical systems exhibit response times orders of magnitude slower than electronic controls (milliseconds vs microseconds), rendering them ineffective for dynamic detuning compensation.

To address these challenges, we designed and implemented an LLRF system capable of adjusting the rf frequency without modifying the reference source or

mechanical tuner during the powering up and rf conditioning. It achieves this by introducing a frequency offset with 95.3 Hz precision within a ± 1.56 MHz range to the reference signal. Based on the relative phase between the pickup and cavity input signals, a phase-locked loop (PLL) feedback module [7] locks the rf frequency to the dynamically varying resonant frequency. This closed-loop control eliminates the need for manual adjustment of either the reference source or the cavity tuner. The LLRF system also integrates other functions to streamline operation: (1) resonant frequency localization, (2) field control for stable power delivery, (3) breakdown protection with rapid power interruption, and (4) real-time waveform graphical display.

This paper first presents the hardware and firmware design, along with the key modules implemented. It then details the low-power test, high-power platform, and series of experiments, with a particular focus on the frequency tracking process. Finally, the conclusion is presented.

II. HARDWARE AND FREQUENCY MODULATION

This LLRF system was designed to be a versatile platform, catering not only to the experiments in this paper but also to potential requirements in other facilities. This forward-looking approach explains why some of its capabilities may appear nonessential for the current specific application. In the interest of a clear and streamlined narrative, a detailed discussion of the redundant design considerations is omitted here.

Figure 2 depicts the LLRF system. The shell is a 6-slot CPCI chassis equipped with a 5-inch screen, where a CPU board communicates with two digital boards via the PCIe protocol. Each digital board interacts with its respective

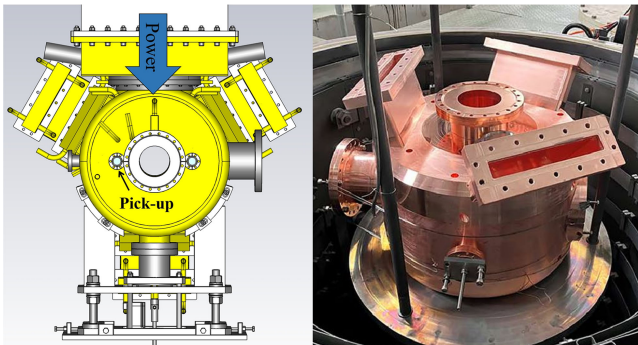


FIG. 1. Mechanical model and picture of rf cavity.

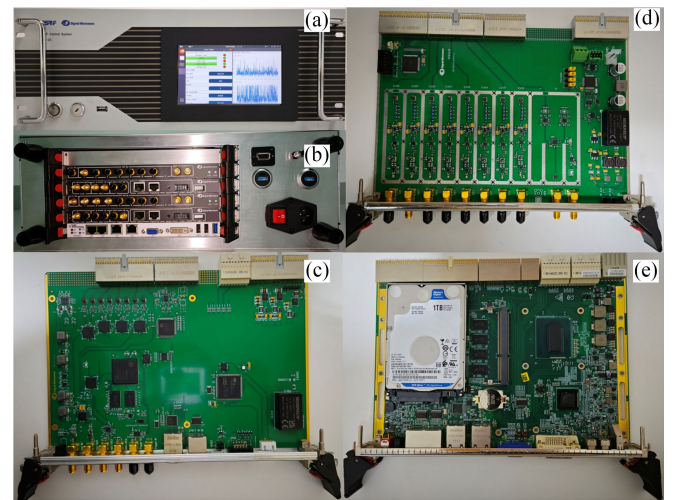


FIG. 2. LLRF system components: (a) front panel; (b) back panel; (c) FPGA-equipped digital board; (d) 8-channel front-end board; and (e) CPU board.

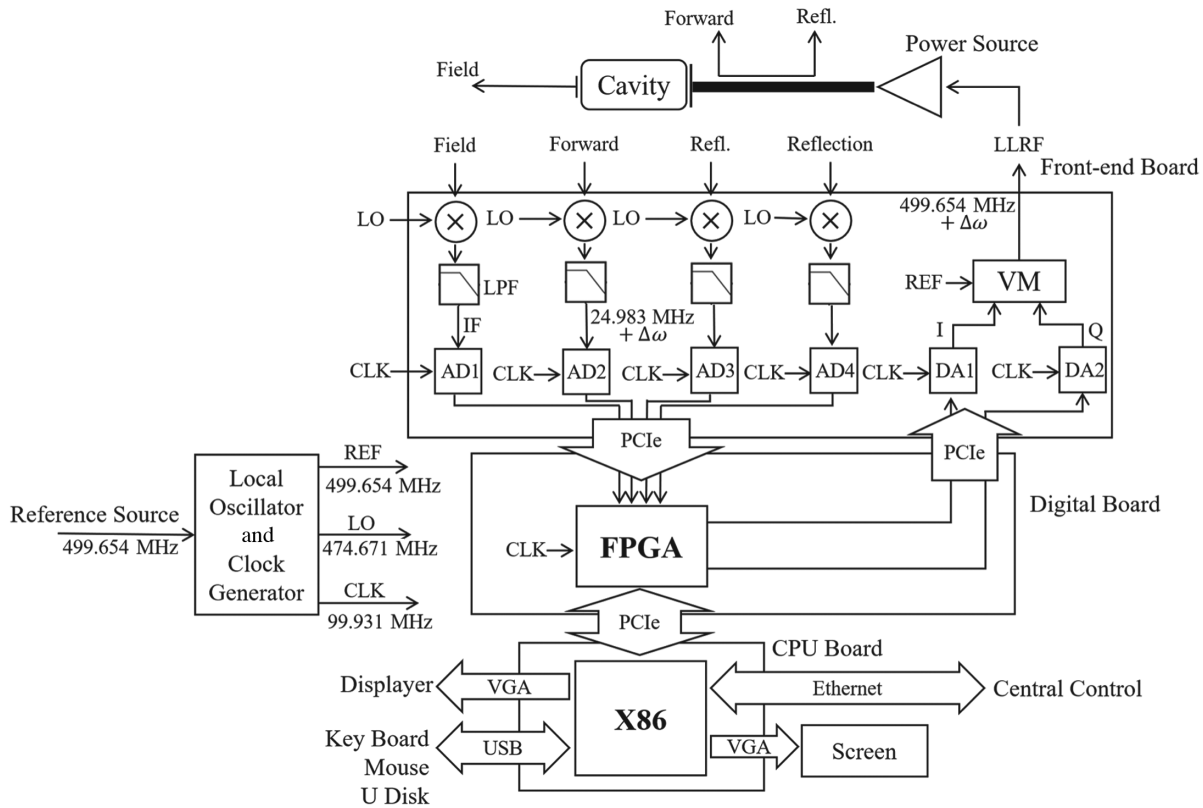


FIG. 3. Hardware and devices illustration.

front-end board through the backplane bus. Additionally, each front-end board features eight rf-in channels and a single rf-out channel. For this platform, only one digital board and four rf-in channels are utilized.

The rf signals must first be converted into digital values to enable algorithmic processing. As illustrated in Fig. 3, the local oscillator and clock generator produce three phase-locked signals derived from the fractional frequency of the reference source (Rohde and Schwarz SMW200A). Simultaneously, the cavity field, forward wave, reflected wave, and LLRF output are mixed with the LO signal before being sent to the low-pass filter (LPF). The rf signal is down-converted to the intermediate frequency (IF), which is equal to the difference between the pick-up signal and the LO. The IF is then sampled by a 16-bit analog-to-digital converter (ADC). Following this, the FPGA (Xilinx XC7A100-2TFGG484 SoC) processes the ADC information to compute optimal outputs for the 16-bit digital-to-analog converters (DACs). Additionally, the same clock signal synchronizes the ADCs, FPGA, and DACs for global timing.

During cavity power-up, the rf frequency must track the shifting resonant frequency without modifying the reference source or cavity tuner. This requirement necessitates the vector modulator (VM) [8] capable of simultaneously adjusting the amplitude, phase, and frequency of the reference signal, as illustrated in Fig. 4. Unlike traditional methods that rely on direct-current (dc) signals, the VM

uses two orthogonal, equal-amplitude sinusoids to control the rf signal's third dimension. Furthermore, a calibration module within the FPGA ensures that the amplitude and phase errors of these analog sinusoids are maintained below 0.19% rms and 0.18° rms [9], respectively. Notably, frequency modulation is activated only in the powering-up stage, so frequency errors smaller than the cavity bandwidth are tolerable. Additionally, the CPU board is equipped with a processor (Intel i7-4700) and universal peripherals, enabling it to operate independently as a standalone computer.

The CPU board operates on the Ubuntu graphical operating system. The Experimental Physics and Industrial Control System (EPICS) [10] is employed to define and broadcast process variables (PV) mapped to FPGA registers, enabling comprehensive monitoring and control of the LLRF system through PV access from both

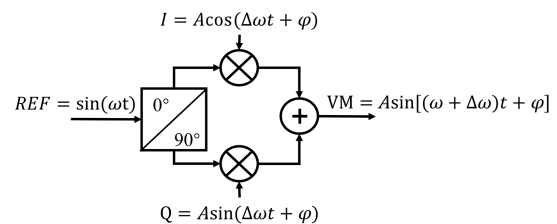


FIG. 4. VM model and frequency modulation mechanism.

the CPU and external systems. Additionally, a user-friendly graphical interface (GUI) is developed with PyDM [11].

This architecture offers significant flexibility by distributing functions across different processing units based on their specific requirements. Tasks demanding high real-time performance are implemented in the FPGA, while those requiring frequent modifications or extensive interaction with external systems are handled by the CPU. Computationally intensive operations that necessitate very large resources are managed at the central control level.

III. FIRMWARE

The below firmware is entirely implemented in the FPGA. To achieve a balance between performance and resource utilization, multiple timing domains are created by dividing the CLK by 2^n . These domains are phase-locked to the same clock and operate at integral multiples of each other, allowing data to be transmitted between domains without the need for caching. For the slow module receiving fast signals, a random sample within each long cycle is selected to represent the signal. Conversely, the fast module performs oversampling of the slow signal. The preceding explanation provides the necessary foundation for the following detailed analysis. An overview of the

complete firmware architecture is presented in Fig. 5, with detailed descriptions provided in the corresponding subsections.

A. Parameters configuration

The necessity for real-time LLRF tuning during facility operation is addressed by a system design that facilitates on-the-fly reconfiguration of FPGA modules through dedicated register access. The CPU and FPGA exchange data through direct access to a shared memory block. A configuration table systematically distributes parameters to individual registers, enabling real-time module adjustments. Concurrently, waveform data are packed into predefined memory segments at a rate of 10 Hz. This architecture allows the operating system to display real-time device status and rf channel metrics.

B. LLRF output modes

The operation of an accelerator requires distinct control logic at different stages, making it essential to switch swiftly and reliably between these modes. During high-power testing, the LLRF system must fulfill three critical functions: (1) rapidly disabling rf stimulation to protect components in case of faults, (2) maintaining amplitude and phase stability

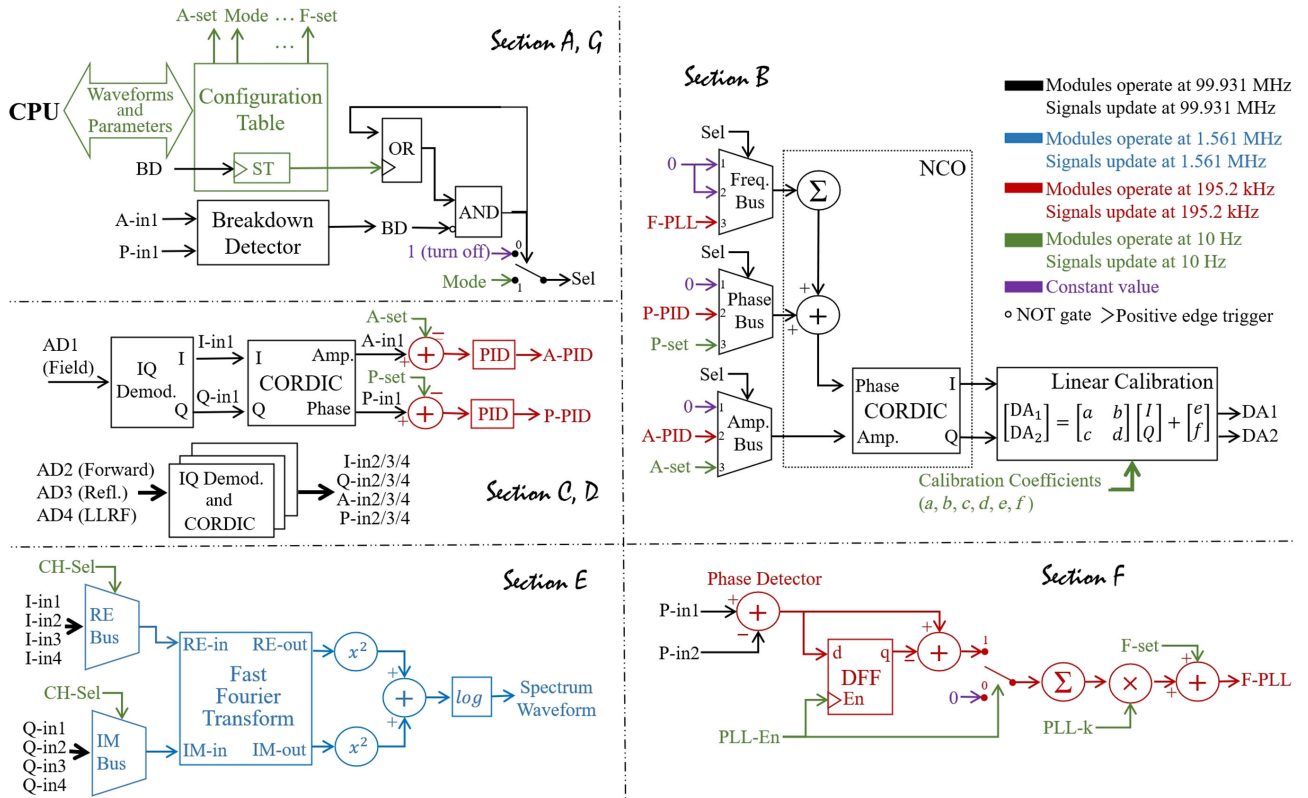


FIG. 5. Firmware architecture in FPGA. (Color coding distinguishes modules or signals operating or updating within distinct frequency-timing domains. Detailed explanations about modules are provided in the following corresponding subsections).

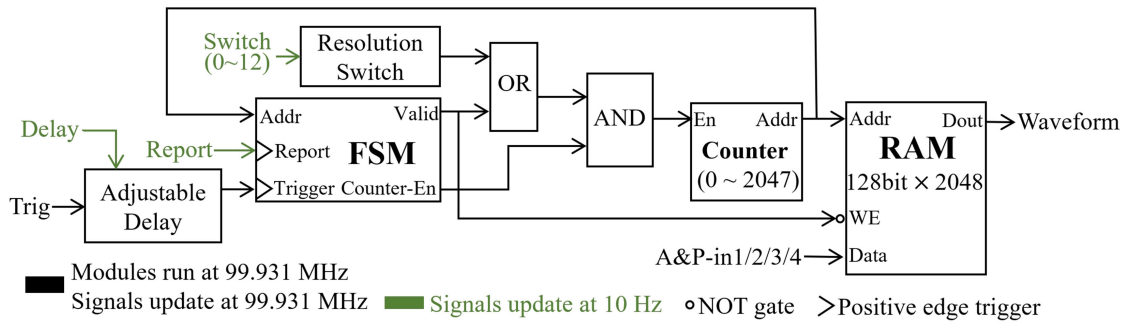


FIG. 6. Multiresolution waveform recorder.

against slow drift during extended operation, and (3) tracking the resonant frequency dynamically during rf power ramping. Accordingly, the LLRF system is designed to operate in one of these modes based on specific operational requirements.

Three multiplexers function as centralized control buses, consolidating signals from various functional modules. Each multiplexer routes a selected input directly to its output based on the Sel signal, enabling the system to operate in three modes, as illustrated in Fig. 5: *Mode 1* (off-state): A Sel value of 1 initiates a protective shutdown that rapidly zeros the rf amplitude while maintaining full operational readiness of all other modules, guaranteeing seamless reactivation. *Mode 2* (beam acceleration): A Sel value of 2 activates dual proportional-integral-derivative (PID) controllers to stabilize the rf amplitude and phase during beam acceleration. In this mode, the frequency bus outputs zero, enabling the VM to be driven by dual dc signals. As a result, the LLRF output frequency remains phase-locked to the reference source, ensuring strict synchronization with the beam. *Mode 3* (powering-up/conditioning): A Sel value of 3 activates the PLL controller to track the resonant frequency during cavity charging or rf conditioning procedures.

When the frequency bus outputs a nonzero value, the phase input of the Coordinated Rotation Digital Computer (CORDIC [12]) varies periodically and linearly, generating dual digital sinusoids with a 90° phase shifted and equal magnitude. These sinusoids introduce a frequency offset—determined by the frequency bus output—to the reference within the VM. A calibration module compensates for hardware-induced amplitude and phase mismatches, ensuring that the dual analog sinusoids produced by the downstream DACs maintain 90° phase quadrature and equal magnitude.

Phase control is implemented using 17-bit signed fixed-point numbers, covering a $\pm 180^\circ$ range with a resolution of $360^\circ/2^{17} \approx 0.03^\circ$. Frequency tuning utilizes a 15-bit signed fixed-point representation, combined with a 20-bit cycle accumulator that increments at each CLK. The accumulator's upper 17 bits are summed with the phase setting, achieving a resolution of $99.931 \text{ MHz}/2^{20} \approx 95.3 \text{ Hz}$ and a tunable range of $\pm 95.3 \text{ Hz} \times 2^{14} \approx \pm 1.56 \text{ MHz}$.

C. Waveform extraction

The in-phase and quadrature (I/Q) components are demodulated from the sampled rf signals of each channel. These components are then converted into polar coordinates using pipelined CORDIC modules, concatenated into a single data word for recording, and finally transmitted to the CPU for decoding. This enables real-time waveform visualization on GUI.

However, the cw system presents a significant challenge, as the FPGA generates waveform data at hundreds of GB/s—a rate that precludes full real-time recording and plotting. Therefore, a multi-resolution acquisition strategy is implemented, wherein waveform data are recorded at a time resolution dictated by operator demand. The architecture of this firmware design is depicted in Fig. 6.

1. FSM-based waveform recording architecture

Data words are buffered in a block of random access memory (RAM) within the FPGA pending retrieval by the CPU. A finite state machine (FSM) manages the counter and the RAM to facilitate waveform recording. The state transition diagram for this FSM is presented in Fig. 7. The system operates through a cyclic addressing mechanism: a counter cycles continuously from 0 to 2047, generating sequential addresses that correspond to the 2048 memory locations in RAM. Each address stores a single data word.

2. State transition logic

Initially, the FSM is in the Update state. Data are written continuously and circularly to the RAM, with the oldest

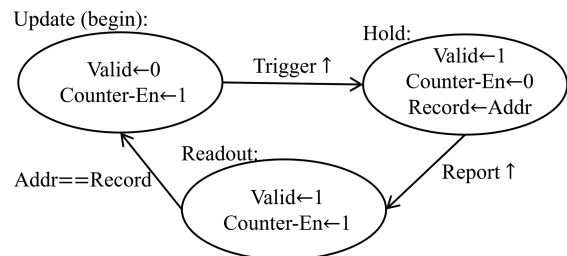


FIG. 7. State transition diagram of the FSM in Fig. 6.

entries being overwritten by the newest data, effectively maintaining a rolling buffer of the most recent 2048 samples.

Recording is finished by a trigger signal. Upon detecting a rising edge (a transition from low to high) on the external Trig input, the FSM transitions to a new state. The counter halts, and its current value is saved into a Record register. This stored value serves as the start address pointer for the captured waveform segment. The Delay signal in Fig. 6 adjusts the arrival time of the Trig signal, controlling the position of the observation window relative to the external trigger event. The FSM then asserts a Valid output signal to indicate that the requested waveform data are ready in RAM and awaits an acknowledgment.

Finally, upon receiving the Report signal from the CPU, the system enters a Readout state. In this state, the counter counts through 2048 addresses starting from the Record pointer, outputting the waveform data. Once the readout process is complete, the FSM returns to its Update state.

3. Multiresolution recording

The Switch register allows for online adjustment of the waveform resolution. This register accepts an integer value between 0 and 12. The Resolution Switch module uses this value to control data recording rates. It generates a single-clock-wide pulse (logic high) every 2^{Switch} clock cycles and remains at logic low otherwise. When Switch is set to 0, the module outputs a constant logic high, enabling data capture on every clock cycle. This module is only active during the Update state of FSM. In this state, a new data word is recorded into RAM only when the Resolution Switch module pulses high, down-sampling the data by a factor of 2^{Switch} . During the subsequent Readout state, the entire set of 2048 words stored in the RAM is transmitted over 2048 clock cycles, regardless of the Switch setting. This ensures a consistent data output frame. This multiresolution approach enables the system to cover a wide range of time scales. The observable time resolution can be adjusted from $2^0/99.931 \text{ MHz} \approx 10 \text{ ns}$ (when Switch = 0) to $2^{12}/99.931 \text{ MHz} \approx 40 \mu\text{s}$ (when Switch = 12), with a corresponding time window ranging from $10 \text{ ns} \times 2048 \approx 20 \mu\text{s}$ to $40 \mu\text{s} \times 2048 \approx 80 \text{ ms}$.

D. PID controller

The fundamental requirement for the LLRF is to maintain rf power stability against slow drift during beam acceleration. To achieve this, two independent PID controllers [13] regulate the amplitude and phase of the rf field around their predefined setpoints. Given the rf-loop delay of approximately $3 \mu\text{s}$ in our platform, all feedback modules operate on a subclock driven at $1/512$ of the main clock. This subsampling strategy effectively absorbs the loop delay, enabling rapid LLRF response while avoiding oscillations.

E. Spectrum analyzer

The axiom that “a craftsman cannot create what he cannot measure” applies to rf systems: since an LLRF system is capable of generating a frequency-offset rf signal, it must also be capable of measuring that frequency. To fulfill this requirement, a real-time fast Fourier transform (FFT) module [14] is implemented to acquire the frequency and signal-to-noise ratio (SNR) for each channel. The FFT processor updates the spectrum using a 4096-point data buffer at $1/64$ of the CLK, achieving a frequency resolution of $\frac{99.931 \text{ MHz}}{4096 \times 64} \approx 382 \text{ Hz}$ across a $99.931 \text{ MHz}/64 \approx 1.561 \text{ MHz}$ span centered at the reference frequency. The spectral results are converted to logarithmic scale and encoded as 9-bit integers with 4-bit fractional precision. This design achieves an accuracy of 0.2 dB within a 90 dB range without requiring a logarithm lookup table. A shared FFT core is used to minimize resource usage, with all channel signals routed to it through two multiplexers.

F. PLL controller

During rf conditioning and powering-up, the cavity frequency will continuously change, so the PLL controller aims to track the change. It primarily comprises a numerically controlled oscillator (NCO) and a phase detector, which together with the rf cavity constitute the phase-locked loop. The system leverages a key phenomenon: the relative phase between the pickup signals and cavity input monotonically decreases as the resonant frequency drops, a variation that is most pronounced near resonance. This characteristic enables the loop to lock the relative phase at a predetermined value.

Operational details: (1) Initial Frequency Evaluation: Determine the frequency difference between the resonant frequency and the rf signal monitoring the cavity’s reflected magnitude or impulse response. (2) Frequency Offset and Phase Locking: Set the frequency offset and enable the PLL-En register. The rising edge of this register triggers a data flip-flop (DFF), capturing the current relative phase as the feedback target. The PLL-k parameter fine-tunes the loop gain, optimizing system performance. (3) Frequency Tracking: As the cavity temperature fluctuates, the real-time relative phase is locked to this target. The PLL continuously adjusts the rf frequency, maintaining synchronization with the cavity resonance.

G. Breakdown protection

To protect against rf breakdown, a detector monitors the reflected wave. Once the wave’s amplitude exceeds a predefined threshold for a specified duration, the circuit triggers a breakdown warning signal (BD) by switching its logic level from low to high. This signal immediately sets the Sel value to 1, activating the LLRF output off-state (described in Sec. III B).

Simultaneously, the status register (ST) latches the warning as an active-low signal. It is triggered by the

rising edge of BD and remains latched until explicitly cleared by the CPU. This interlock ensures the warning state cannot be exited without explicit acknowledgment.

IV. LOW-POWER TEST AND VERIFICATION OF FREQUENCY MODULATION

First of all, to validate the accuracy of the frequency modulation, the LLRF output is simultaneously analyzed using both its integrated spectrum analyzer and a commercial

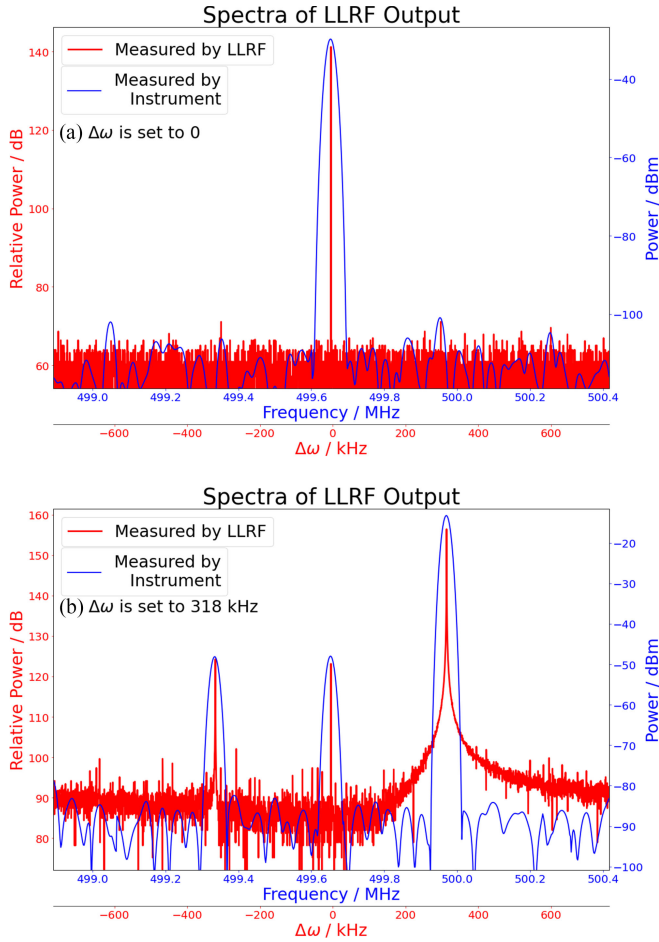


FIG. 8. LLRF output spectra measured by the built-in analyzer and external instrument prior to calibration. (a) Synchronized operation: LLRF output frequency matches the reference source frequency. (b) Frequency offset test: LLRF output frequency is shifted by +318 kHz relative to the reference. Harmonic distortions emerge under non-synchronized conditions. (The built-in analyzer's X axis represents relative frequency deviation ($\Delta\omega$) from the reference frequency, while its Y axis displays normalized amplitude. In contrast, the external instrument's X axis shows absolute frequency (in MHz), and its Y axis measures absolute power (in dBm). Despite these differing parameter definitions, the two coordinate systems share identical scale divisions (units per axis division). Furthermore, the X axis is calibrated such that $\Delta\omega = 0$ (zero frequency offset) aligns precisely with the reference frequency of 499.654 MHz, ensuring direct comparability between relative and absolute frequency measurements).

external instrument (Rohde and Schwarz FSWP50). As illustrated in Fig. 8(a), the built-in analyzer resolves spectral components that match the external instrument's measurements. The spectral component captured by the LLRF exhibits minimal bandwidth, a result of phase synchronization between all FPGA module clocks.

Further validation is performed by introducing a frequency offset of 318 kHz. As demonstrated in Fig. 8(b), the built-in analyzer retains accurate spectral resolution. The observed bandwidth arises from quantization error inherent to the digital system, which introduces nonidealities in the LLRF output during frequency modulation. Notably, harmonic distortions emerge when the rf frequency deviates from the reference source frequency.

The harmonic observed at the reference frequency originates from dc bias in the DACs, while the symmetric harmonic component arises from crosstalk between the I/Q signal paths and gain mismatch between the paired DACs. To mitigate these distortions, a multivariable parameter estimation algorithm [9] is employed. Since these errors exhibit linear system behavior, the correction coefficients can be derived using input-output data pairs. A feedforward calibration module then applies these coefficients to pre-distort the digital sinusoids, compensating for the hardware nonidealities prior to DAC transmission. As shown in Fig. 9, this approach suppresses harmonics, achieving a clean output. In addition, this process introduces a method to detect and calibrate amplitude and phase crosstalk.

And then, the LLRF output is coupled to the rf cavity, while the pickup and input signals are monitored to derive the frequency-dependent gain and phase drift. Frequency scanning around the resonant frequency is performed by independently tuning the LLRF system and reference

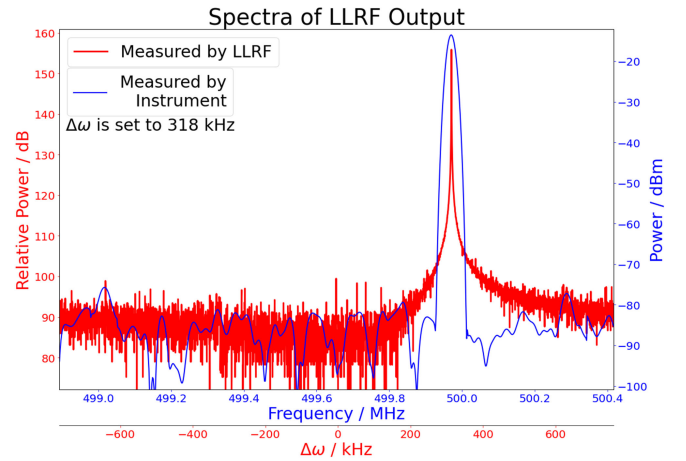


FIG. 9. Calibrated LLRF output spectra measured by the built-in analyzer and external instrument. Harmonic distortions identified in Fig. 8(b) are suppressed following calibration. The plot configuration (axes definitions, scale divisions, and measurement parameters) aligns with Fig. 8 to ensure consistent analytical comparison.

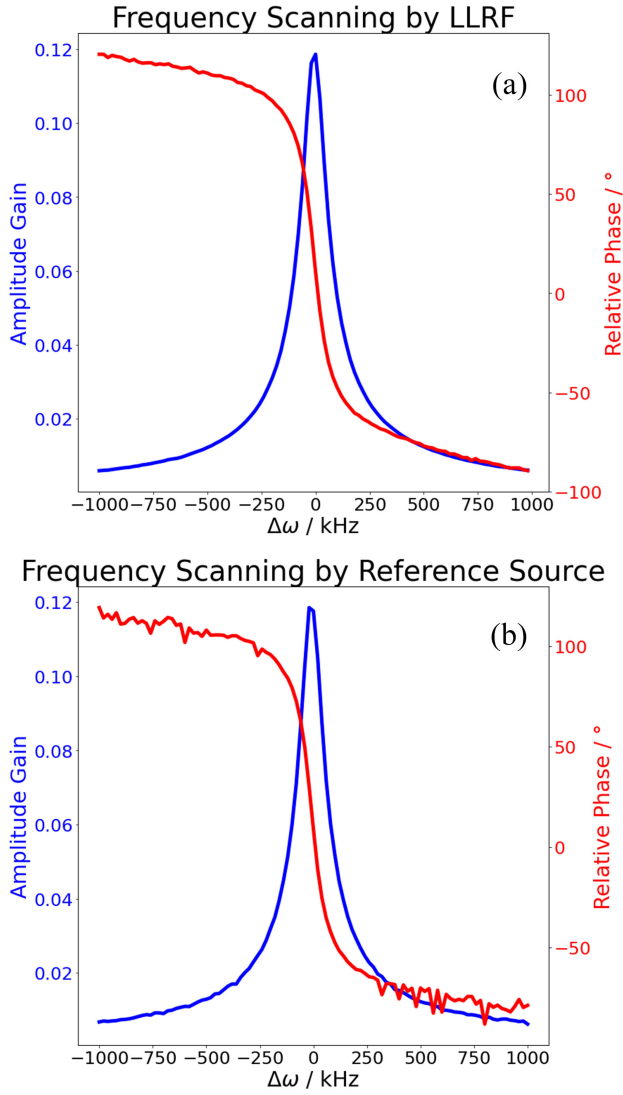


FIG. 10. Frequency response of the rf cavity under two measured methods. (a) LLRF scanning: The reference source is locked to the cavity's resonant frequency, while the LLRF system sweeps the frequency offset ($\Delta\omega$) over a ± 1 MHz range to measure detuning effects. (b) Reference source scanning: With $\Delta\omega$ fixed at 0 (no offset), the reference frequency itself is continuously swept across the resonant.

source. As illustrated in Fig. 10, the cavity's distinct resonant peak and characteristic 180° phase shift are clearly resolved. Furthermore, the LLRF-driven frequency adjustment demonstrates superior smoothness and linearity compared to the reference-based method, confirming the LLRF's precision in frequency modulation.

V. HIGH-POWER PLATFORM AND RF CONDITIONING

Prior to deployment in operational facilities, rf systems must undergo rigorous rf conditioning and performance validation. To enable this, a high-power rf test platform

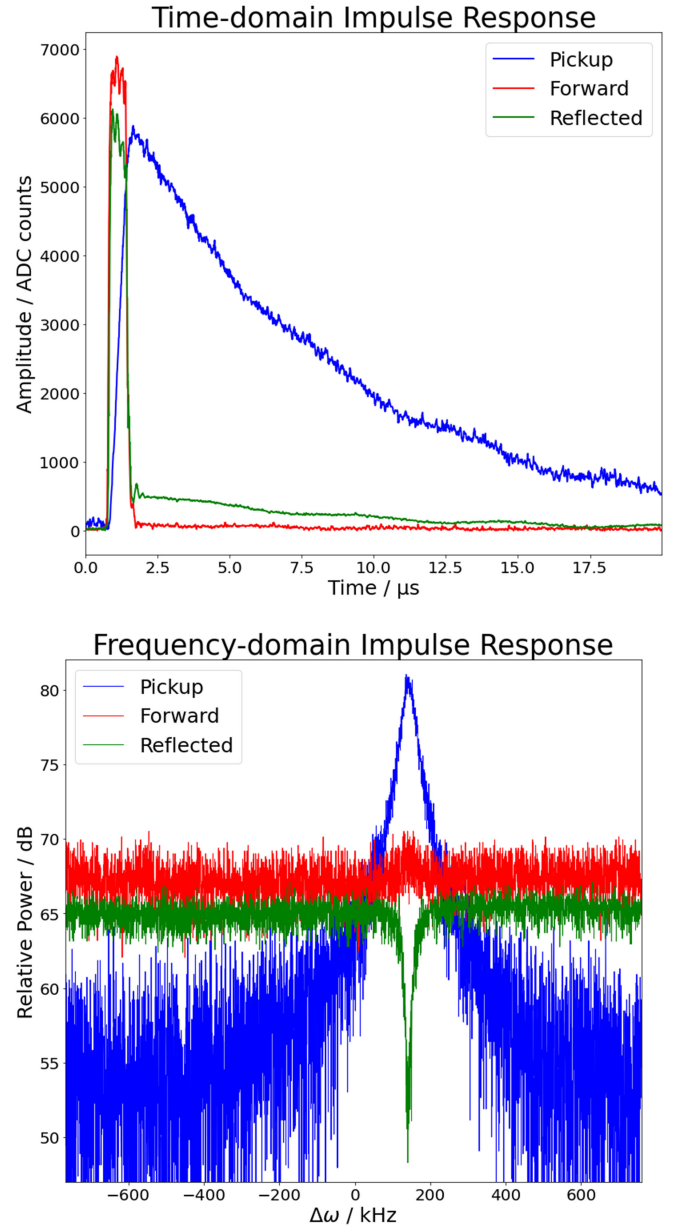


FIG. 11. Cavity impulse response in both time-domain and frequency-domain, measured by the LLRF. (The waveforms are computed directly from ADC samples, resulting in normalized amplitude and power values without physical units. Furthermore, direct quantitative comparisons between different curves are not valid, as the rf measurement channels exhibit distinct attenuation levels).

has been developed. The system utilizes a commercial reference signal, with the LLRF providing closed-loop control of the power source. The platform supports cw operation at power levels up to 50 kW. A directional coupler, installed upstream of the rf cavity, enables monitoring of forward power, reflected power, and pickup signals via the LLRF system. This configuration ensures precise characterization of cavity behavior and detection of anomalies

during high-power testing. Additionally, the central control room nearby can regulate the entire platform.

A. Location of resonant frequency

Before energizing the rf cavity, frequency matching between the rf source and the cavity's resonant frequency is critical to avoid destructive reflected power. For linear time-invariant (LTI) systems, the frequency response corresponds to the Fourier transform of the time-domain impulse response [15]. Leveraging this principle, the cavity's resonant frequency is determined by analyzing the pickup signal spectrum while exciting the cavity with a short LLRF-producing pulse approximating a delta function.

In this implementation, the FPGA-integrated spectrum analyzer operates at a sampling rate of 1.56 MHz. A $1/1.56 \text{ MHz} \approx 640\text{-ns}$ rf pulse is used as the deltalike excitation signal. A 4096-sample spectral waveform is generated, resulting in a pulse duty cycle of $1/4096 \approx 0.024\%$. Such pulses do not risk damaging the rf system. As illustrated in Fig. 11, the resonant and reflected peaks coincide at the same frequency. In contrast, the spectrum of the forward wave exhibits a nearly flat profile. The initial cavity detuning of 150 kHz can be read out from the spectrum. After applying this frequency offset to correct the rf frequency, high-duty-cycle rf power is safely delivered to the cavity.

The unloaded quality factor (Q factor) of the cavity can be derived from its frequency-domain reflection curve in Fig. 11 [16]. The measured value of 29 631 compares favorably with the design value of 31 880 in Table I, yielding a relative error of 7%. This agreement also corroborates the validity of the resonant frequency measurement method employed.

B. PLL control and frequency tracking

Following low-duty frequency matching, the system initiates the conditioning mode (Sec. III B) to track the cavity's resonant frequency. Figure 12 illustrates the resonant frequency drift during high-power operation. As ohmic losses in the cavity walls increase, the resonant frequency decreases by approximately 200 kHz—exceeding the cavity's nominal bandwidth—when the rf power reaches 50 kW. Concurrently, the PLL controller continuously adjusts the rf frequency to hold the reflected power to 8.5% of the incident power, ensuring stable power delivery. Fluctuations in frequency arise due to environmental changes.

Upon reaching the target rf power level, a residual frequency offset persists between the cavity and the reference source. To compensate for this discrepancy, a remotely operated mechanical tuner on the cavity is activated. Throughout this adjustment process, the LLRF system maintains PLL control until $\Delta\omega = 0$ is achieved,

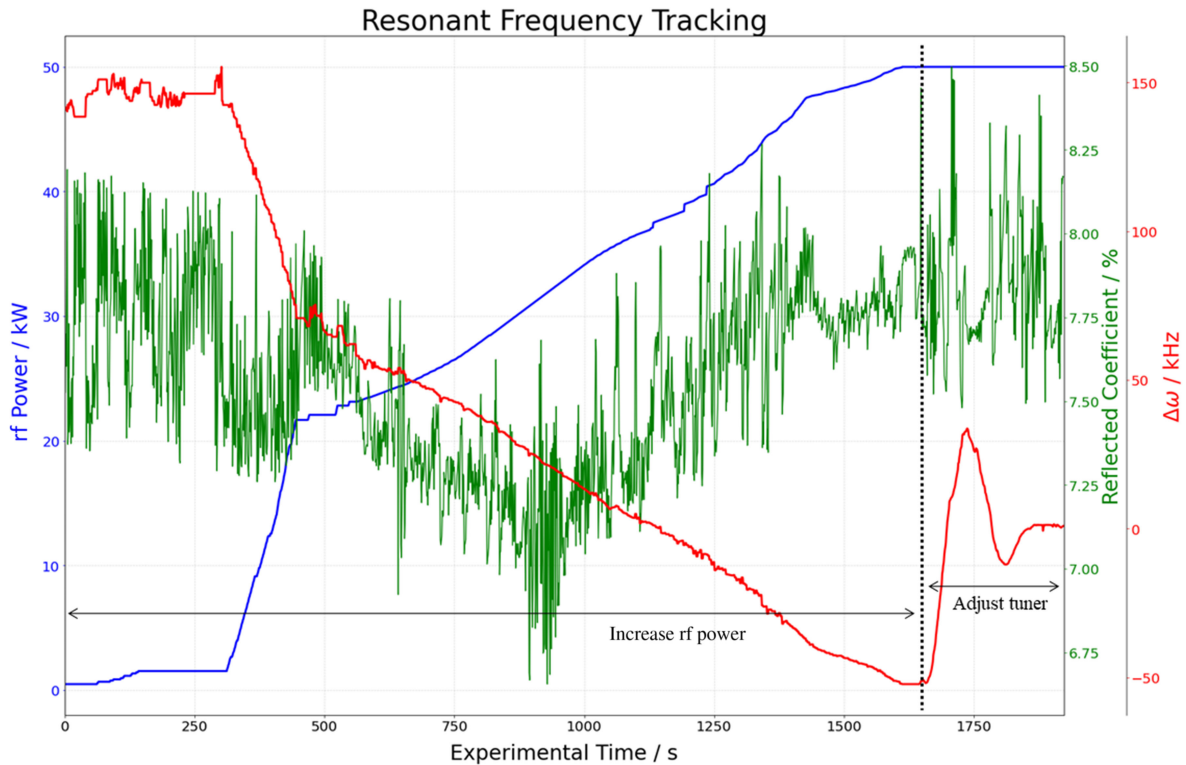


FIG. 12. Resonant frequency tracking during rf cavity operation, performed in two stages: (1) Power ramp-up: Increase rf input power to 50 kW. (2) Tuner calibration: Adjust the tuner to compensate for the residual frequency offset.

indicating that the cavity resonant frequency is locked to the 499.654 MHz reference.

With the cavity fully activated and stabilized, the PLL controller is deactivated, and the frequency offset is reset to zero. The LLRF output frequency is now phase-locked to the reference source, marking the system's readiness for beam acceleration. Throughout the no-beam process, the mechanical tuner is engaged only once. This optimization minimizes mechanical wear, mitigates risks of alignment faults, and enhances operational reliability by reducing dependence on manual interventions.

C. Long-term stability

This experimental validation focused on the system's capability to suppress slow drift, rather than pursuing optimal performance parameters, as it was conducted with a commercial-grade reference source under nonideal environmental conditions. Operating in the beam acceleration mode (Sec. III B) with $\Delta\omega = 0$, the system employed dual PID controllers to independently stabilize amplitude and phase. Over a 24-h test, it effectively restrained slow drift, achieving an amplitude stability of 0.12% (rms) and an additive phase stability of 0.088° (rms) between the reference and pick-up signals. If a high-precision reference or an optimized operational environment, the system has the potential for improved performance.

VI. CONCLUSIONS

An automatic frequency tracking method fully based on a digital LLRF system has been developed for normal-conducting rf cavities. This method employs two orthogonal analog sinusoids of equal amplitude to modulate the reference signal frequency, enabling the LLRF system to achieve an adjustable output bandwidth. To support this functionality, a real-time spectrum analyzer is implemented in FPGA to monitor frequency deviations. Experimental results demonstrate that the system can measure rf signal spectra within a 1.56-MHz bandwidth and generate rf signals with arbitrary frequencies across a 3-MHz bandwidth. Furthermore, the PLL-based frequency tracking process maintains the cavity reflected power below 8.5% of the incident power during power-up and mechanical tuning, ensuring stable power delivery. The design does not require additional devices, offering a compact and flexible solution. It is advantageous for microwave structures that require both compensation for large resonant frequency shifts and precise measurement of the resonant and rf frequencies. Additionally, this PLL-based tracking method can be adapted to beam-loaded operation by replacing VM-based rf frequency adjustment with direct cavity tuner control.

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DATA AVAILABILITY

The data that support the findings of this article are openly available [17].

TABLE II. Abbreviations.

Abbreviation	Full name
ADC	Analog-to-digital converter
CORDIC	Coordinated Rotation Digital Computer
CPCI	Compact peripheral component interconnect
CPU	Central processing unit
cw	Continuous wave
DAC	Digital-to-analog converter
dc	Direct current
DFF	Data flip-flop
EPICS	Experimental Physics and Industrial Control System
ESRF	European Synchrotron Radiation Facility
FFT	Fast Fourier transform
FPGA	Field programmable gate array
FSM	Finite state machine
GUI	Graphical user interface
I/Q	In-phase and quadrature
IF	Intermediate frequency
LLRF	Low-level radio frequency
LO	Local oscillator
LPF	Low-pass filter
LTI	Linear time-invariant
NCO	Numerically controlled oscillator
PCIE	Peripheral component interconnect express
PID	proportional-integral-derivative
PLL	Phase-lock loop
PV	Process variable
PyDM	Python display manager
RAM	Random access memory
rf	Radio frequency
rms	Root mean square
SNR	Signal-to-noise ratio
SSRF	Shanghai Synchrotron Radiation Facility
VM	Vector modulator

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