

First results from a high-frame-rate, multi-GHz ionizing particle detection system geared toward accelerator diagnostic applications

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An integrated detection system, consists of a thin diamond sensor incorporated into a compact signal loop, coupled in turn to an application-specific integrated circuit readout chip, has been tested for the first time, using ps-duration electron pulses from the Next Linear Collider Test Accelerator at the SLAC National Accelerator Laboratory. For readout frame rates as high as 120 kHz, the detection system is shown to achieve a linear dynamic range of 10^3 and a bandwidth of 4–5 GHz, with no ringing seen on the tail of the output pulse. These results represent the best-performing multi-GHz ionizing particle detection system achieved to date.

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I. INTRODUCTION

X-ray free-electron lasers (XFELs) are renowned for their capability to provide high-intensity (mJ scale) pulses of coherent x-rays. However, due to the inherently unstable nature of the underlying lasing process, XFEL beams tend to vary widely in intensity and centroid location from pulse to pulse. To accommodate this, beam diagnostics have been developed that provide pulse-by-pulse measurement of the pulse intensity, to be made use of by beam control systems and experimenters. Particularly effective are diamond-sensor pass-through diagnostic systems that can provide precise pulse-by-pulse characterization of XFEL beam properties at repetition rates of up to 50 MHz [1,2], providing the MHz-scale repetition rate capability required by current XFEL sources.

However, either through population of successive rf buckets of an S-band accelerating structure [3] or through pulse splitting and delay [4], multi-GHz repetition rates are envisioned for future XFEL facilities. The development of

pulse-by-pulse beam characterization diagnostics for such facilities represents a significant challenge: for detection bandwidths above 1–2 GHz, the “rf regime” is encountered, for which electrodynamic effects begin to compromise signal generation, transport, and readout performance, confounding attempts to develop detection systems through the use of standard tools. Thus, a concerted effort to develop high-rate beam diagnostics that can be sensitive to generated signal sizes over a large dynamic range is warranted, motivated by the needs of experiments that can take advantage of knowledge of the intensity and centroid location of each delivered pulse, and for diagnostics that can help to control and optimize the XFEL beam itself. Such a system would also be likely to find application in other fields. For example, the temporal resolution scale associated with a 5 GHz detection bandwidth is approximately 100 ps, commensurate with the 100–150 ps burn width of an inertially induced fusion event [5].

To meet this need, the Advanced Accelerator Diagnostics (AAD) Collaboration, consisting of groups from two University of California campuses and three U.S. National Laboratories, has developed an integrated (sensor, signal path, and readout) multi-GHz detection system as a first step toward a deployable position-sensitive diagnostic that can characterize particle beam properties at GHz repetition rates. This system consists of a novel compact signal path constructed around a biased electronic-grade

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diamond sensor, with a transient signal response of order 100 ps duration, coupled in close proximity to a custom integrated circuit chip [the FastPulse Precision Sampler, or FPS, application-specific integrated circuit (ASIC)] specifically designed to read out pulses from the compact signal path. In July 2025, the integrated detection system was exposed to short-duration (~ 1 ps) bursts of bunches of minimum-ionizing (40 MeV) electrons from the SLAC NLCTA test facility [6], leading to an essentially instantaneous generation of signal charge (electrons and holes) within the diamond sensor, and providing a first test of the performance of the integrated detection system.

This article begins with a description of the components of the integrated detection system, and techniques used in its fabrication, then provides background on the system deployed in the Next Linear Collider Test Accelerator (NLCTA) beam and the acquired datasets, before proceeding to discuss the analysis of the acquired data and the results of the analysis. While aspects of the detection system (signal path and readout) have been described independently in prior publications [7,8], this article presents results for the first time from the integrated detection system, which, to the best of the authors' knowledge, is the best-performing GHz ionizing particle detection system developed to date.

II. GHZ DETECTION SYSTEM

A. Compact signal path

The elements of the compact signal path are depicted in Fig. 1. A semiconductor sensor is affixed directly to the upper surface of an array of commercial “single-layer” capacitors that rests atop a conducting copper plane that serves as an overall ground reference. Signal current is carried by bond wires to the contact of a commercial “back contact” resistor that serves simultaneously as a signal return path and sensing element, and provides damping for oscillations arising from LC resonances within the signal path. Signal pulses (current or voltage, depending upon the amplification scheme of the readout system) are picked off the resistor electrode and carried over additional wire bonds to the readout system—the FPS ASIC for the results presented in this article.

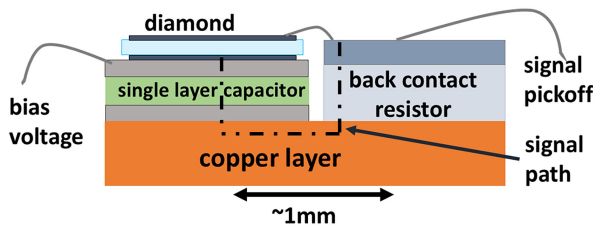


FIG. 1. Elements of the compact signal path. When assembled as described in the text, the lateral and vertical dimensions of the signal current flow are approximately 2.5 and 0.25 mm, respectively. Note that the bias voltage, with polarity as noted in the text below, is applied to the underside of the diamond sensor.

The sensitive element chosen for the system exposed to the NLCTA beam was a metallized CVD diamond sensor fabricated from an electronic-grade substrate produced by the Element Six Corporation [9]. The 4×4 mm², 500 μ m thick substrate was thinned to 31 μ m and diced to a lateral size of 1.9×1.9 mm² by the Applied Diamond Corporation [10]. Planar electrodes, each of dimension 1.6×1.6 mm² and consisting of a 5 nm thick interface layer of Ti overlain with a 50 nm thick Pt conducting sheet, were grown on either side of the thinned substrate using photolithographic techniques, making use of the AAD Collaboration's affiliation with the CINT laboratory [11] in Albuquerque, NM. The resulting capacitance of the fabricated sensor is approximately 4.2 pF.

The choice of diamond as a sensor material was motivated by its fast carrier drift speed (approximately 200 μ m/ns for bias fields above 3 V/ μ m [12]), and its relatively low dielectric constant of 5.7, which limits the capacitive load presented to the readout by the sensor. For comparison, the corresponding values for detector-grade silicon are approximately 100 μ m/ns and 11.7, respectively.

The sensor was affixed to the upper surface of an array of eight 10 pF Knowles Dielectric Labs D30NS100M1BX single-layer capacitors resting on a ground plane of 1 oz (1.4 mil thick) copper. The edge of the capacitor array extends several hundred microns beyond the diamond sensor, allowing the sensor to be biased via a bond wire that connects a high-voltage trace patterned into the ground plane to the upper surface of the capacitor array. Electrical continuity between the capacitor array and diamond sensor was established through a layer of 3M Corporation 5113DTF-50 double-sided electrically conductive tape and between the capacitor array and ground plane through a reflow solder layer. The capacitors were arranged around a circular hole of diameter 500 μ m in the ground plane and supporting printed circuit board to allow for the passage of a particle beam through to the sensor without absorption or degradation. Potting epoxy was applied around and between the capacitors to avoid breakdown between the bottom surface of the sensor and the ground plane. The vertical distance between the surface of the copper ground plane and the upper electrode of the diamond sensor was approximately 200 μ m.

A Vishay Electro-Films IGBRB1000BJANCT5 back contact resistor, of value 10 Ω , was soldered to the ground plane directly adjacent to the sensor and capacitor stack. The back contact resistor is approximately 1×1 mm² wide and 250 μ m thick. Electrical continuity between the resistor and diamond sensor was established with a set of two parallel wire bonds. Beam-induced transient signal current passing through the back-contact resistor created a voltage pulse across the resistor, which was carried out via a bond wire to an input pad of the FPS ASIC. The backplane of the FPS was affixed directly to the continuous ground plane using a layer of silver epoxy. The design specification

TABLE I. Table of measured performance parameters of the FPS ASIC. The effective number of bits (ENOB) is determined from the ratio of the linear dynamic range to the lowest achievable readout noise.

Parameter	Value	Unit
Bandwidth	> 5	GHz
Sampling rate	Up to 37	Gs/s
Capture window	1.25–2.5	ns
Maximum readout rate	> 6	MHz
Maximum slew rate	3.0×10^9	V/s
Linear dynamic range	> 150	mV
Resolution (ENOB)	10	bits

and properties of the FPS ASIC are described in the following subsection.

B. The FPS ASIC

The four-channel FastPulse Precision Sampler (FPS) ASIC was designed by the AAD Collaboration to provide a high-bandwidth, rapid-sample capture of up to 2.5 ns of transient signal response. Measured performance parameters of the FPS ASIC are summarized in Table I. More details about the design and performance of the FPS ASIC can be found in [8,13].

A three-stage front-end transimpedance amplifier (Fig. 2) drives signals onto a 45-element switched capacitor array (SCA) with an adjustable sampling rate. Bench tests performed with external calibration signals and a low input load impedance suggest an analog bandwidth in excess of 5 GHz, consistent with the performance of the overall

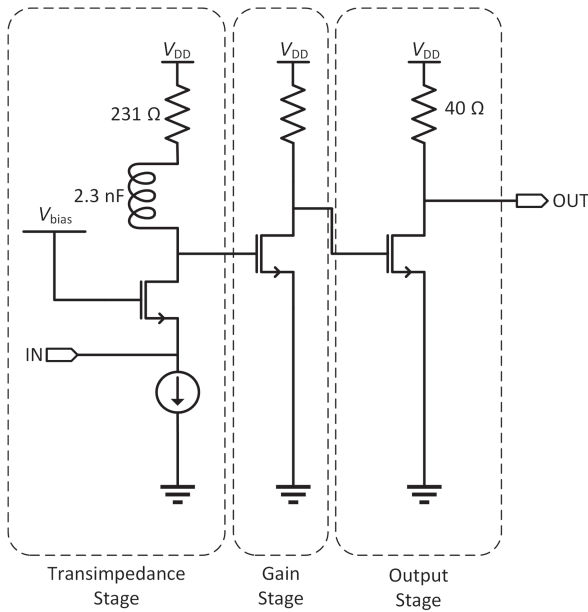


FIG. 2. Schematic representation of the FPS front-end amplifier. The resistor in the gain stage is a variable active PMOS load, controlled by an external current source.

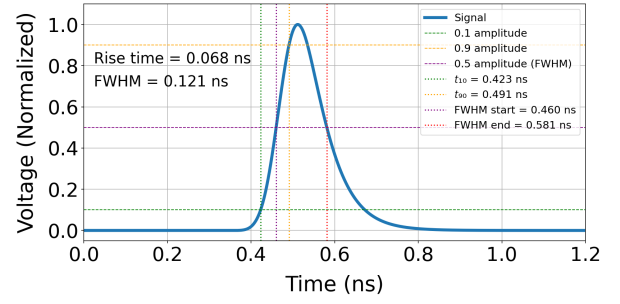


FIG. 3. Simulated response of the FPS ASIC to a signal from the compact signal path of Sec. II. A. The expected signal rise time and full width at half maximum (FWHM) are approximately 70 and 120 ps, respectively.

detection system (signal path, transport to FPS input, amplification, and sampling) described below. Figure 3 shows the simulated response of the FPS to a signal generated within the sensor of the compact signal path described above, for a signal amplitude roughly in the middle of the FPS ASIC's linear dynamic range. The expected signal rise time and full width at half maximum (FWHM) are approximately 70 and 120 ps, respectively.

For the highest sampling rate setting, the sampling period was determined by introducing a calibration pulse from an Agilent 8110A pulse/pattern generator into each of the three channels not used to read out the signal path and measuring the response of each capacitor in the SCA as the calibration signal was delayed in increments of 5 ps. Figure 4 shows the resulting individual capacitor responses for all 45 capacitors in the array for one of the three characterized channels (channel 1). Also shown in Fig. 4 are the delays corresponding to the 50%-of-maximum crossing times for each capacitor (vertical lines), which are plotted as a function of capacitor number in Fig. 5. The slope of the line in Fig. 5 provides the additive inverse of the sampling period, yielding a sampling period estimate of 27.1 ± 0.3 ps averaged over the three characterized channels. This corresponds to a sampling rate of 36.9 ± 0.4 Gs/s.

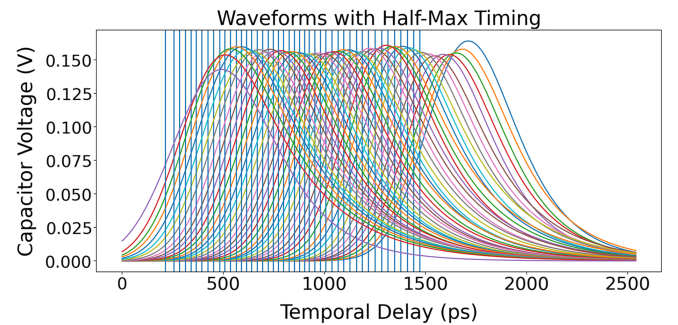


FIG. 4. Response of each capacitor in the Channel 1 SCA to a calibration pulse, as a function of pulse delay. The vertical lines represent the 50%-of-maximum crossing point of each signal.

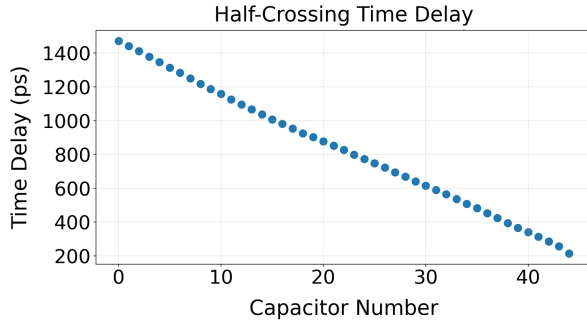


FIG. 5. Plot of the 50%-of-maximum crossing points from Fig. 4 as a function of capacitor number. The slope of the line yields the additive inverse of the sampling period.

The response of the FPS amplifier/driver system has been found to be linear to approximately 160 mV, with a saturation limit of 250 mV [8]. After an acquisition, the SCA voltages are held until a readout phase begins, in which the voltages in the SCA are presented one-by-one to an output pad of the FPS ASIC, in response to an external readout clock whose frequency (“readout rate”) can be accommodated over a wide range of values. Studies of the performance of the FPS readout for clock rates as high as 6 MHz are presented below.

C. Integrated detection system

A picture of the assembled detection system, including the compact signal path and FPS readout ASIC, is provided

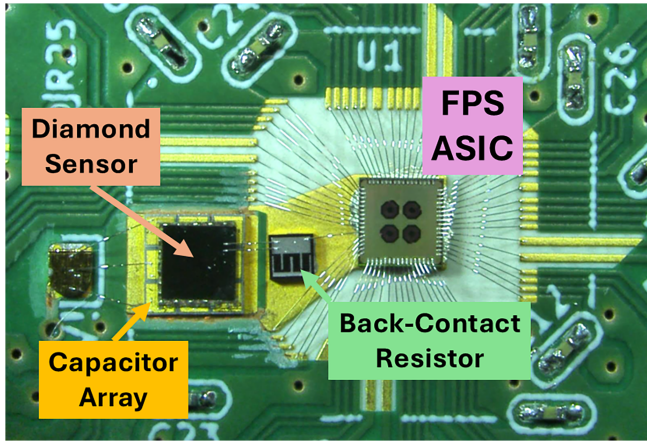


FIG. 6. Micrograph of the assembled detection system, including the compact signal path and FPS readout ASIC, on its carrier PC board. The diamond sensor, affixed to the top of an array of eight single-layer capacitors, is seen left of center. The beam strikes the diamond sensor perpendicular to the surface of the diamond sensor visible in the picture (into the page). A through-hole of 500 μm diameter was drilled in the open space in the middle of the capacitor array, just below the middle of the diamond sensor, to allow for the passage of a focused beam. The back contact resistor is immediately to the right of the sensor, and to the right of the resistor, and in the center of the photograph, is the FPS ASIC with its pattern of bond wires associated with its triggering, control, calibration, and readout.

in Fig. 6. The detection system is mounted on an eight-layer “carrier” PC board, with the top and bottom dielectric layers formed from 4-mil thick Rogers 4350 Material [14]. The internal layers of the carrier board are uninterrupted ground plane, connected through vias to the top metal ground reference.

High-bandwidth 50 Ω traces carry a differential trigger and a calibration signal from the periphery of the board to the appropriate input pad of each of channels 1–3 of the FPS ASIC; for channel 0, which is used to read out the signal path, only a differential trigger signal is provided. Lower-bandwidth traces carry the readout clock to each ASIC channel, provide dc analog levels that establish the ASIC operating point, and carry the clocked analog output from each channel’s SCA to an analog devices AD8003ACPZ buffer amplifier. As the channel’s SCA is clocked out, its amplifier drives the acquired SCA voltage levels into coaxial cables that carry the signals away from the vicinity of the beam, to be digitized and stored.

III. THE NLCTA RUN AND DATASET

A. The NLCTA test system

To operate the detection system in an accelerator beam environment, the system’s control must be interfaced to the accelerator’s timing system. A photograph of the fully interfaced NLCTA test system is shown in Fig. 7. At the front of the assembly is the carrier board that houses the detection system (shown in expanded view in Fig. 6). Immediately behind the carrier board is a “control” board that provides conditioned low voltage for the operation of the carrier board and translation between single-ended signals from an external Raspberry Pi (RPI) control module and the low-voltage differential signaling (LVDS) logic protocol used by the FPS ASIC. Bias voltage for the diamond sensor is introduced directly onto the carrier board

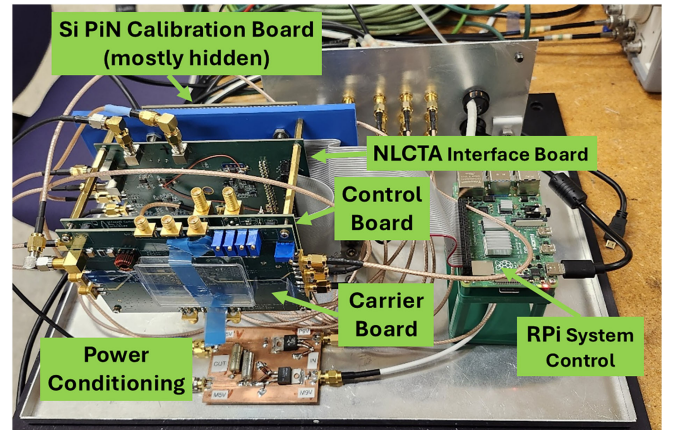


FIG. 7. Photograph of the NLCTA test system. The plastic cover on the carrier board protects the detection system during handling and was removed before directing the beam onto the diamond sensor.

through an SMA input connected to a filtered trace that carries the bias level to the upper surface of the capacitor array. Signals from the SCA output drivers of each of the four channels of the FPS ASIC (only one of which is made use of for the NLCTA beam studies described here) are routed through the control board to an “interface” board, described below. Electronic connectivity between the carrier and control boards is provided by four rigid board-to-board connectors near each of the four corners of the boards, which also serve as mechanical stand-offs between the two boards.

Approximately 10 cm behind these two interconnected boards, the interface board provides a translation of a timing signal from the NLCTA into the LVDS protocol required to trigger the FPS acquisition window. The interface board also houses four AD8003ACPZ buffer amplifiers that drive the SCA voltage levels from each FPS channel out to SMA connectors on the back panel, to which cables can be attached that carry the signals away from the beam enclosure. The interface board splits the timing signal into two separate high-speed trigger paths, one of which is routed to the trigger input of the FPS ASIC, and the other of which is routed directly to an output SMA connector, to provide a timing reference for operation in the NLCTA beam. It also provides a copy of the NLCTA trigger to the RPi, as an instruction to initiate the FPS readout after a suitable delay. Electronic connectivity between the forward (carrier and control) system and the interface board is established through a 32-conductor ribbon-cable connection between the control and interface boards.

A final PC board, containing a $2 \times 2 \times 0.05$ mm³ single-pad silicon PiN diode sensor, sits immediately behind the interface board, allowing the timing of the NLCTA beam pulse to be measured, to sub-ns precision, relative to the timing reference signal. The relative delay between a signal generated by the PiN sensor and the arrival of a trigger signal at the FPS ASIC, as represented by the timing reference signal, was measured in the Santa Cruz Institute for Particle Physics (SCIPP) laboratory to 1–2 ns precision. All boards in the four-board series contain a hole of at least 500 μ m diameter to minimize disruption of the passing beam.

The FPS readout clock is provided by the commercial RPi system, acting in slave mode relative to the NLCTA timing pulse. The RPi system also provides an interface to the test system user, allowing multievent runs to be initiated and FPS control levels to be set remotely through an ethernet connection.

B. Operation in the NLCTA beam

The system was controlled from a bunker just outside the accelerator enclosure, in which timing signals from the NLCTA accelerator were available. Communication between the bunker and test system was done through RG58 coaxial cables; to circumnavigate the shielding wall, these cables were required to be 45 m long. The outputs of

the AD8003ACPZ buffer amplifier connected to channel 0 of the FPS (the channel that read out the signal path), and the readout start and clock signals from the RPi module, were connected through these cables to the inputs of a Keysight Infiniium UXR0134A digital storage oscilloscope, configured to digitize and record these outputs with 1 GHz bandwidth.

The accelerator timing signal was routed from a patch panel in the control bunker to the input of an Agilent 8110A Pulse/Pattern Generator, which relayed the timing signal after a delay adjustable in multiples of 5 ps. The delayed timing signal was routed to the interface board of the NLCTA test system through another of the 45 m cables, providing the source of the trigger for the FPS acquisition window and the associated timing reference signal.

Knowing the delay of the PiN signal relative to the timing reference signal to within 1–2 ns, and making use of the adjustable delay of the pulse/pattern generator to tune the relative timing of the beam pulse and FPS trigger, allowed for the test system to be synchronized with the NLCTA beam prior to biasing the diamond sensor and enabling the FPS readout. The diamond was then biased, and the FPS readout was enabled with its sampling rate set to its lowest value, providing a 2.5 ns window for the initial observation of the beam signal in the detection system. Once the signal was observed, the sampling rate was set to its maximum value of 37 Gs/s and the pulse/pattern generator delay was adjusted to center the NLCTA pulse in the minimal-duration (1.22 ns) FPS acquisition window. Figure 8 shows an example of the detection system’s response to a single NLCTA pulse, at the maximum sampling rate of 37 Gs/s, clocked out at a readout rate of 2 MHz.

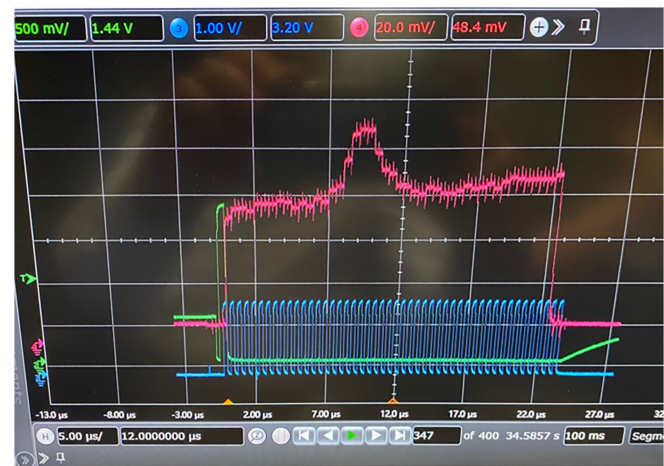


FIG. 8. Acquired oscilloscope readout of a typical NLCTA pulse. The green trace is the enable signal from the RPi control module, which initiates the 2 MHz readout clock (blue trace). The magenta trace displays the voltage levels observed on each of the 45 SCA capacitors, acquired at the maximum sampling frequency of 37 Gs/s, with the vertical scale set to 20 mV per division.

C. Accumulated dataset

Signals were first observed, and data collected, in the afternoon of July 16, 2025. Data were accumulated at the 10 Hz repetition rate of the NLCTA accelerator, in 400 pulse blocks (runs) each at the maximum sampling rate of 37 Gs/s. Data were acquired for various values of the diamond sensor bias voltage (+50, +100, +150, +200, and −100 V) at a readout clock rate of 2 MHz, and at a bias voltage of +200 V with readout clock rates of 4 and 6 MHz. Pedestal runs, with the beam stoppered to ensure no signal was generated within the diamond sensor, were interspersed within the data taking. Five pedestal runs were taken during the 2 MHz running, and one each for the 4 and 6 MHz runs.

For each pulse of each run, the clock (blue trace in Fig. 8) and SCA readout (magenta trace in Fig. 8) were written to disk. In any given run, the maximum observed SCA voltage level (peak height) varied widely from pulse to pulse, from near 0 to as much as 250 mV.

IV. ANALYSIS AND RESULTS

A. System response

Given the design parameters of the FPS ASIC and the known properties of electronic grade diamond sensor material, it is possible to estimate the system response, in terms of signal peak height in mV per fC of delivered minimum ionizing (beam) charge.

In a 30 μm thick diamond, a minimum-ionizing electron loses approximately 20 keV of kinetic energy to ionization processes [15]. Accounting for the mean pair-creation energy of 13.3 eV [16], this yields approximately 1500 signal charges, all of which will be collected promptly by an undamaged electronic grade diamond sensor. For an instrument response function of 125 ps (4 GHz), this generates a peak total signal current I_t of order 2 μA . The signal current divides itself between the 10 Ω return path and the 62 Ω input impedance of the FPS ASIC [13], yielding a peak signal current into the front-end transimpedance amplifier of

$$I_{\text{TIA}} = \frac{I_t}{1 + \frac{62}{10}} \cong 0.28 \mu\text{A}.$$

Given the expected FPS transimpedance of 250 Ω [13], this yields an expected signal response of approximately 70 μV per delivered beam electron. A 150 mV peak signal response thus corresponded to a delivered charge of approximately 2150 electrons or about 0.35 fC. This value lies well below the threshold of the NLCTA bunch charge diagnostic system, but comfortably within the range of the PiN sensor included in the test system (Fig. 7), allowing the NLCTA beam to be monitored using the PiN sensor output. However, during the operation of the test system, the beam traversed a significant air column between the

vacuum exit window and the test system, expanding it to several centimeters in diameter and introducing significant and widely varying showering of the part of the beam that did not strike the diamond sensor. As a result, little correlation was observed between the PiN and FPS outputs, making the PiN sensor (which was included primarily for the purpose of providing a timing reference for the enabling of the FPS acquisition window) an unreliable measure of the total delivered signal charge. Thus, the PiN diode traces were not recorded, and no confirmation of this estimated response could be provided by the accumulated data. As a final note, a delivered charge of 0.35 fC of beam electrons would generate a signal charge (number of electron-hole pairs excited) within the diamond sensor of approximately 0.5 pC.

B. SCA data reduction

As can be seen in Fig. 8, the digitized SCA voltage levels were impacted by clock transition pickup, scope digitization noise, and the rise time of the signal as it is driven onto the long cables between the accelerator housing and the control room. A sample time trace for several capacitors, with an expanded timescale, is shown in Fig. 9. A stable region is seen both before and after the ringing in the middle of the traces caused by crosstalk from the readout clock transition. The four vertical lines form the temporal boundaries of two bands over which the trace is integrated to average out readout noise. For each NLCTA pulse, the sampled voltage for each capacitor is taken to be the average value of the trace within these two temporal bands. For the pedestal runs with a 4 and 6 MHz readout clock, the regions over which the SCA voltage level is averaged are correspondingly shorter in time.

C. Pedestal, dynamic range, and frame rate

A capacitor-by-capacitor average pedestal value can be formed for each of the pedestal runs by averaging the sampled voltage level, derived as described above, over the 400 acquisitions in the run. The results of this procedure,

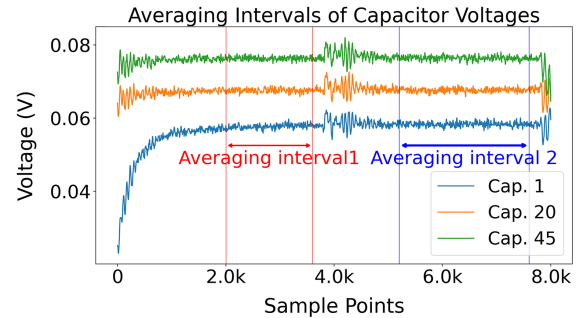


FIG. 9. Sample time trace for several capacitors, for one event from a pedestal run with a 2 MHz data readout clock. The four vertical lines form the temporal boundaries of two bands over which the trace is integrated to average out readout noise.

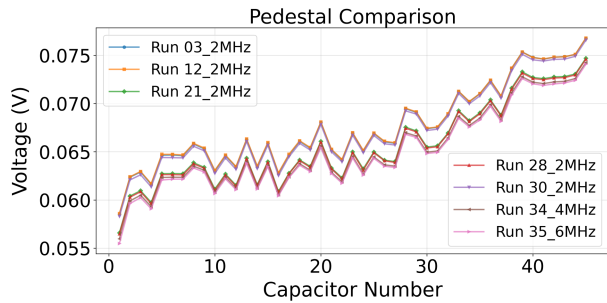


FIG. 10. Mean sampled voltage level for each capacitor in the SCA, for each of the seven pedestal runs.

for each of the seven pedestal runs, are shown in Fig. 10. This figure shows a consistent dependence of the pedestal upon capacitor number, with a drift of the overall pedestal level on the order of ± 1 mV.

By calculating the rms deviation of the SCA voltage around its mean, for each capacitor in the array, an upper limit on the SCA sampling noise can be determined. This rms value is uniform within $\pm 10\%$ from capacitor to capacitor. For the 2 MHz readout, this rms value was generally between 135 and 150 μV over the 45 capacitors in the array for three of the five pedestal runs and between 180 and 190 μV for the other two pedestal runs, with the difference likely due to the drift of the overall pedestal level during the acquisition period for the two runs with the larger rms values. For the 4 MHz pedestal run, the rms values were generally between 180 and 195 μV , while for the 6 MHz pedestal run, the rms values were generally between 190 and 205 μV .

Given the FPS linear range of ~ 160 mV [8], the 2 MHz sampling noise figure of 135–150 corresponds to a linear dynamic range in excess of 10^3 or an effective number of bits (ENOB) of greater than 10. A 2 MHz clock rate through the array of 45 elements in the SCA leads to a readout time of 22.5 μs , implying a frame rate of approximately 40 kHz. The sampling noise observed for 4 and 6 MHz readout was slightly higher (180–200 μV), but some or all of the difference could be attributable to pedestal drift rather than sampling noise. Regardless, the pedestal data show that the detection system can be operated with a linear dynamic range of close to 10^3 at frame rates up to 120 kHz. Furthermore, the limitations in the frame rate arose from the clock pickup (oscillations observed in Fig. 9) and the limited response speed caused by the load imposed by the long (45 m) cable run. Neither of these is intrinsic to the FPS ASIC itself, and so with further attention to its implementation, even higher frame rates maintaining the 10^3 dynamic range are likely possible.

D. Response to NLCTA beam pulses

For acquisitions in which NLCTA beam pulses impinged upon the diamond sensor, the sample capacitor voltages

were again determined from the acquired oscilloscope traces in the manner described above. For each acquisition, an average of the first eight samplings was used to estimate an overall offset, which was subtracted from each sample in the trace. The resulting traces for single acquisitions for pulses from the low (12 mV peak height), intermediate (75 mV peak height), and high (147 mV peak height) portions of the linear range of the FPS ASIC, as well as one from the saturated regime (236 mV), are shown in Fig. 11. The diamond sensor was biased to +200 V for these three acquisitions. The results shown are for a readout clock speed of 2 MHz. Data taken with readout clock speeds of 4 and 6 MHz yielded detection system responses very close to those of the 2 MHz results. The slew rate observed at the 50% crossing point of the largest (236 mV peak height) pulse is approximately 3.0×10^9 V/s.

Figure 11 suggests that the response of the integrated detection system is somewhat dependent on the magnitude of the charge generated in the diamond sensor by the NLCTA beam pulse. To explore this further, each trace from the +200 V runs was fit to a function formed from the convolution of a Gaussian and an exponential function, with the width of the Gaussian, the scale of the exponential, and the mean and height of the convoluted function left as free parameters in the fit. Figures 12 and 13 show the resulting 10%–90% rise time and FWHM, respectively,

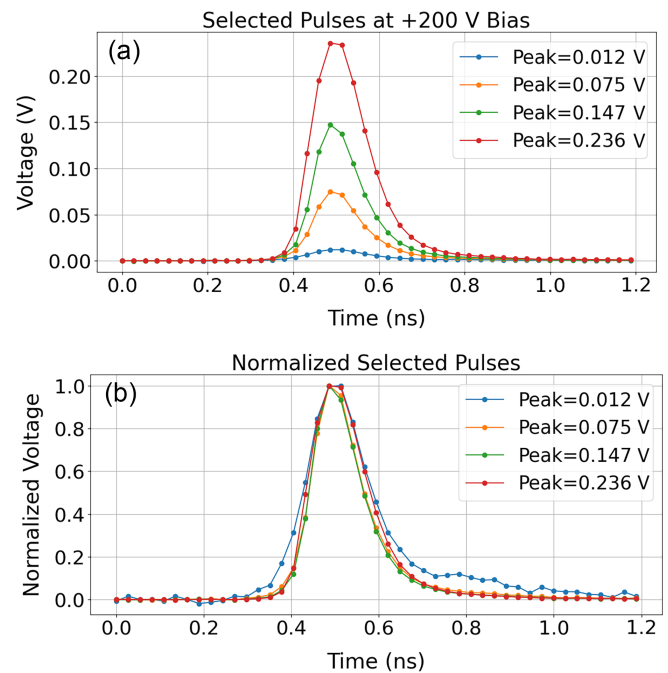


FIG. 11. Absolutely (a) and relatively (b) normalized pedestal-subtracted traces for single acquisitions for pulses from the low (12 mV peak height), middle (75 mV peak height), and high (147 mV peak height) portions of the linear range of the FPS ASIC, as well as one from the saturated regime (236 mV). The diamond sensor was biased to +200 V for these four acquisitions.

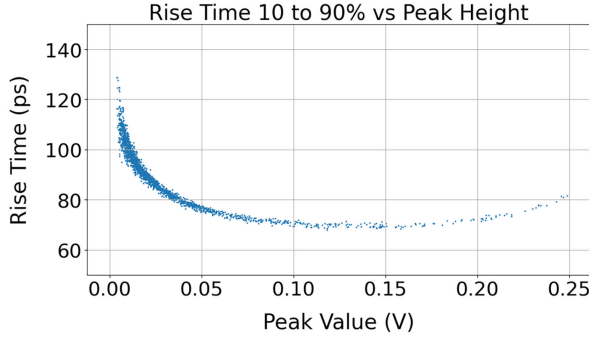


FIG. 12. 10%–90% rise time as a function of peak height, for an applied bias voltage of +200 V.

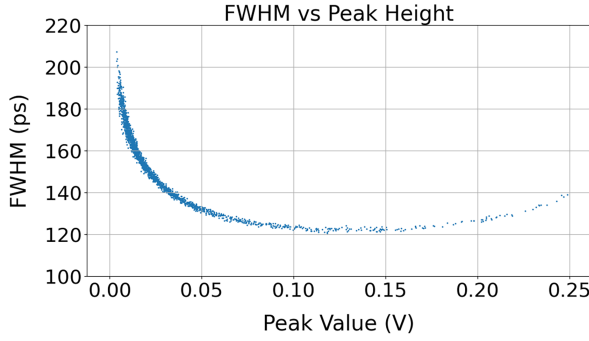


FIG. 13. Pulse full width at half maximum (FWHM) as a function of peak height, for an applied bias voltage of +200 V.

derived from each of these fits, as a function of peak height. Best performance is achieved within a range of roughly 80–200 mV.

Average traces for bias voltages of +50, +100, and +200 V, for pulses with peak height in the range 110–160 mV, are shown in Fig. 14. For bias voltages of +150 and −100 V, no pulses exceeded 100 mV, so corresponding results for those bias voltages are not available. Table II displays the corresponding bandwidth data (10%–90% rise time and FWHM) for these three bias voltages in this pulse-height range. The performance is seen to improve slightly with increased bias voltage, suggesting that even better performance might be observed

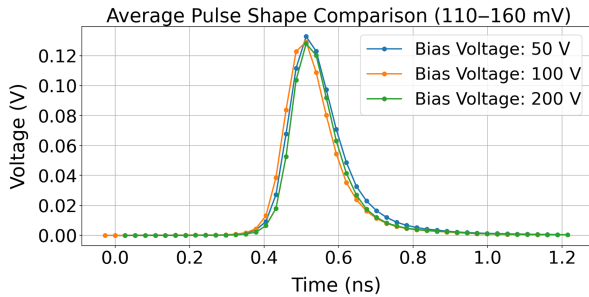


FIG. 14. Average traces for applied bias voltages of +50, +100, and +200 V, for peak heights in the range 110–160 mV.

TABLE II. Observed bandwidth response of the integrated detection system for different applied bias voltages, for peak height between 110 and 160 mV.

V_{bias} (V)	τ_{10-90} (ps)	FWHM (ps)
+50	76	136
+100	74	129
+200	70	122

for a bias voltage above 200 V. Given that the drift speed at 200 V bias (electric field magnitude of 6.5 V/ μm) is expected to be well within its saturated regime [12], though, this seems somewhat unlikely, so the performance at a bias of +200 V is felt to be representative of the best achievable performance of the detection system. The best observed values of risetime (70 ps) and FWHM (122 ps) are very close to those expected from the simulation (68 and 121 ps, respectively).

Using the approximate relations

$$BW = \frac{0.35}{\tau_{10-90}}$$

for a step-function pulse and

$$BW = \frac{0.49}{\text{FWHM}}$$

for a Gaussian pulse, these rise time and FWHM results yield bandwidth (BW) estimates of 5.0 GHz (10%–90% rise time of 70 ps) and 4.0 GHz (FWHM of 122 ps), respectively, for this optimal operating zone.

This quality of this performance significantly exceeds that of existing XFEL diagnostics, which only reach bandwidths of 10 s of MHz [1,2]. The highest bandwidth ionizing particle detection system that the authors are aware of, the DANTE diagnostic system developed for characterizing the burn characteristics of inertial confinement fusion implosion events [17,18], has achieved an analog bandwidth of 2.5 GHz, with an 8-bit effective dynamic range, and is beset by significant oscillations on the falling edge of its output pulse. With its clean pulse response, analog bandwidth of 4–5 GHz, and 10-bit effective dynamic range, the system reported here appears to be the best-performing high-bandwidth ionizing particle detection system built to date.

V. CONCLUSION AND OUTLOOK

By making use of a compact signal path assembled from commercial rf electronic components, and an ASIC developed to read out such a structure, a step forward in the speed and cleanliness of high-bandwidth ionizing particle detection has been made. Performance in the range of 4–5 GHz over a 1.25 ns capture window, with no

electronic ringing observed after the pulse and a linear dynamic range of 10^3 , was demonstrated in a pulsed electron beam. Operation in the optimal region of the system's performance yielded an instrument response function (FWHM) of 122 ps, and the capability to resolve features (10%–90% rise time) at the 70 ps scale, both in good agreement with the design simulation, while achieving frame rates in excess of 100 kHz. This performance establishes this system as the best-performing high-bandwidth ionizing particle detection system developed to date.

As a final note, the observed sampling noise $\sigma_V \approx 140 \mu\text{V}$, in combination with the maximal slew rate $S_{\text{max}} = 3.0 \times 10^9 \text{ V/s}$, leads to an electronic jitter contribution to the timing capabilities of the detection system of order

$$\sigma_t^{\text{jitter}} = \frac{\sigma_V}{S_{\text{max}}} \approx 50 \text{ fs}.$$

This value degrades linearly with decreasing pulse height down to about 50 mV, below which the degradation accelerates due to the observed increase in rise time.

Looking into the future, the group plans a test of a quadrant (position sensing) system in summer 2026. In this second study, the test system will be operated within a vacuum enclosure that allows a focused (few mm diameter) beam to be directed onto the diamond and PiN sensors. This should significantly improve the correlation between the PiN and diamond signals, likely allowing for a pulse-by-pulse determination of the NLCTA pulse charge. The group will also seek support to continue to develop the detection system, with several directions in mind: development of “plug and play” features that will improve the usability of the system for nonexpert groups, a redesign of the FPS ASIC geared toward preserving its intrinsic timing capabilities, adding additional FPS features such as internal digitization and a self-triggering mode that will increase its range of applications; and advancement of the signal-path/preamplifier co-design technique to enable an increase in the overall system bandwidth to as much as 10 GHz.

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DATA AVAILABILITY

The data that support the findings of this article are openly available [19].

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